January 1995
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ELEKTOR ELECTRONICS

THE INTERNATIONAL
ELECTRONICS MAGAZINE

Focus on: Debugging PCs

AUDIO & HI-FI • COMPUTERS & MICROPROCESSORS • DESIGN IDEAS • RADIO, TELEVISION & COMMUNICATIONS • SCIENCE & TECHNOLOGY • TEST & MEASUREMENT

MINI AUDIO DAC

Communications in the Eurotunnel

Quasi analogue clockwork

Dolby surround sound: what is it?

Maxim voltage references

Self-loading EEPROMS

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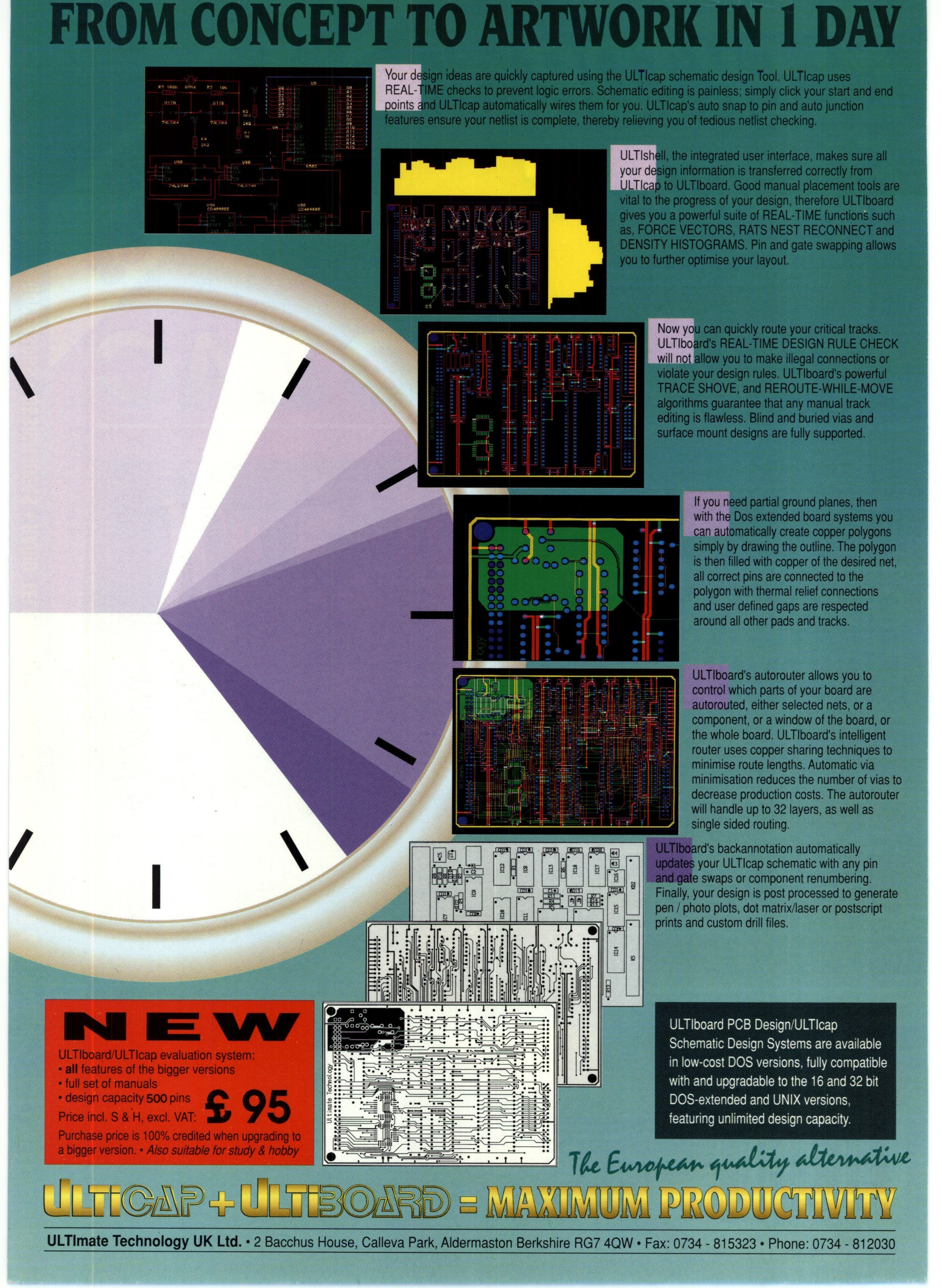

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- Dolby surround processor
- MIDI multiplexer
- MOSFET inverter
- The op amp revisited
- Parameters of RF amplifiers
- and others for your continued interest.

Front cover
The photograph shows a digital-to-analogue converter which is intended to be connected directly to a compact disc player or digital cassette recorder. A special feature of the unit is the possibility of feeding its clock signal to the digital sound source to prevent the conversion causing any jitter. Including the power supply, it is contained on a printed-circuit board rather smaller than eurocard size.

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A B C
AUDIT BUREAU OF CIRCULATIONS
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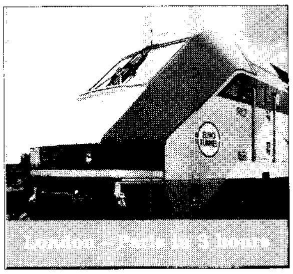

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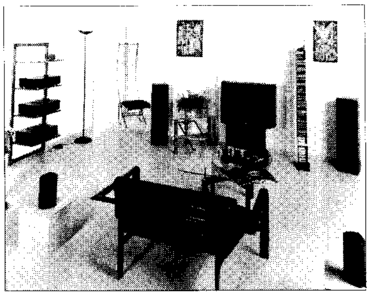

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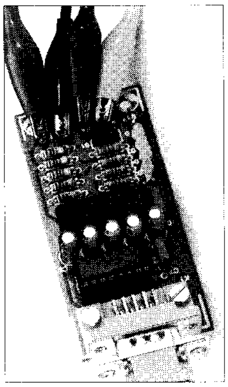

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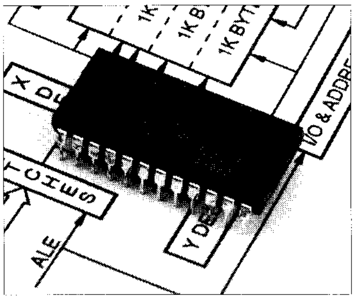

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470	£0.21	£0.24	£0.69	–	–
1000	£0.33	£0.40	£1.05	–	–
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COMMUNICATIONS IN EUROTUNNEL'S HOSTILE SUB-SEA ENVIRONMENT

EuroTunnel, running 91 m below the waves of the English Channel, is the seabed umbilical which has finally reconnected Britain to Europe after a severance of many thousands of years.

There are three tunnels, each 25 km long, linking Cheriton near Folkestone in the UK and Coquelles, near Calais, in France. Two running tunnels are for trains, and a service tunnel for maintenance staff and maintenance vehicles, which can also provide an emergency evacuation route.

The two terminals have large rail loops with loading and unloading platforms. Shuttle trains which are 750 m long operate at 140 km/h through the tunnel and circulate the loops at the terminals, providing a continuous service for transport of cars, coaches and lorries.

Tourist wagons

The shuttle trains are made up of rolling stock which comprises HGV (heavy goods vehicles) wagons, and double or single-deck Tourist Wagons. International freight and passenger trains between London and continental destinations traverse the tunnel at 160 km/h.

The complexity of operating a major utility of this magnitude has made heavy demands on the design of the communications equipment required for the enterprise. In December 1989, the Anglo-French construction company, Trans-Manche-Link (TML), awarded the channel tunnel communications contract to Motorola Land Mobile Products Sector (LMPS), based at Basingstoke in southern England.

Dedicated team

The considerable scope of the TML communications requirement to be met by Motorola necessitated the setting up of a dedicated channel tunnel team at Camberley near Basingstoke, which was supplemented by a hardware and software design group located at Copenhagen in Denmark. The combined teams have been working closely with TML to design, develop, manufacture and maintain systems designed to operate for 20 years.

Five integral radio systems are involved; this article is concerned primarily with the concession radio system and the shuttle internal radio system, both of which were designed at Camberley.

The five systems comprise:

1. **Concession radio**.
   Designed at Camberley and manufactured at LMPS headquarters, this system provides general communications for terminals in the UK and France and both running and service tunnels.
2. **Track-to-train radio**.
   Designed in Denmark and manufactured at Basingstoke, these radios provide communications between the shuttle train driver and control centres in the UK and France.
3. **Paging**.
   Manufactured by the Motorola Paging and Wireless Data Group in Boynton Beach, Florida, the paging system provides communications for management and maintenance personnel in UK terminal areas.
4. **Shuttle internal radio**.
   Designed at Camberley and manufactured at Basingstoke, this system provides a VHF link to car FM radios and on-board driver to captain.
5. **Radiating cable** (leaky feeder).
   This comprises 300 km of tuned UHF cable, of French manufacture, installed in the running and service tunnels and shuttle vehicle. It acts as an antenna for the transmission and reception of radio signals from track to train and concession trunked system, while another application is for the shuttle internal radio.

Design guidelines

System reliability and security were prerequisites in the design parameters adopted. Redundancy in design and architecture was an overarching requirement with duplication of all major items of control equipment, in such a way that radio access is available at any site if a failure occurs. To this end, the track-to-train system uses a hot standby configuration with one controller in the UK and the other in France. The Concession System design arranges that each radio base station is connected to two separate trunk controllers.

The transmission system bearer network interface has been arranged to support this philosophy and architecture as evident in the alternate connection of 'odd' and 'even' base stations and the use of alternating base transmission frequencies on the Concession System.

A number of issues arose owing to the complexity of frequency planning and different usage by the UK and France of the UHF band as well as blocking and intermodulation problems caused by close proximity of equipment in the tunnel environment. These were resolved after prolonged discussion of the plan.

Tough specification

All equipment designed for use in the EuroTunnel has to meet severe environmental criteria. These are much akin to those naval equipment must sustain in tropical usage and imply a marine climate with high humidity and a saline atmosphere. Temperatures may approach 35 °C with high humidity in the equipment rooms towards the centre section of the tunnel system.

In consequence, equipment racks have been fabricated from 2.5 mm marine-grade stainless steel, while all radio and ancillary equipment is fully sealed against ingress of dust and metallic particles, particularly from brake shoes, the necessity for adequate ventilation of units having been taken fully into consideration.

The vibration requirements apply not just to on-board equipment but also to trackside equipment which will be affected by the continual passage of trains at up to 160 km/h. Protection is needed to counter the very high electromagnetic field created by the shuttle locomotives, which is in excess of the normal operating RF/EMC (electromagnetic compatibility) environment of radio equipment and is similar to that specified for military equipment.

Particular attention has been paid to earth bonding of equipment and the introduction of EMC/RFI (radio frequency interference) filters in all control lines to radio base station. All major items of control and radio equipment have therefore been tested against IEC (International Electrotechnical Commission) specifications and ETSI (European Telecommunications Standards Institute) Res 9 guidelines.

Fire hazard

The considerable experience gained from operation of London Underground has brought to the project an awareness of the dangers of fire hazard in underground systems. Therefore, a high degree of fire retardency and halogen-free materials have been specified for all exposed equipment and cabling.

The Concession Radio System, which is based on a conventional multi-site, multi-channel MPT1327 trunked radio system, provides general communications in all three tunnels for operations and maintenance staff and to despatchers in the UK and France rail control centres.

The staff are equipped with hand portable transceivers and provide a back-up system for the EuroTunnel train drivers; they are also fitted in the shuttle terminal transport vehicles that operate in the service tunnel.

Control channels

Therew are two separate control channels available at each base station. Each supports a number of traffic channels providing both speech and data communication between operations and maintenance hand portables, and to the control centres, and speech between mobiles and portables and the PABX (private automatic branch exchange) network and also outbound PSTN (public switched telephone network) connections.

The types of speech call supported are: individual speech calls, group speech calls, group broadcast calls, despatcher calls, PABX calls and outbound PSTN calls. The data calls supported are: status calls, despatcher data calls and mobile text messages.

The architecture of the Concession System divides it into three areas: the UK Terminal (one base site); the Tunnel Zone, incorporating all three tunnels; and the French Terminal (three base sites).

There are 35 radio base station sites each serving all three tunnels. Each radio base station comprises two sections, each controlled via the bearer network from separate trunk controllers to provide redundancy. In the terminal areas, the base stations use conventional antennas, whereas in each of the three tunnels each base station is connected to the leaky feeder.

A tunnel site serves a 1500 m tunnel section and is linked separately, via bearer circuits, to trunk controllers in both the French and UK terminals. Odd-number tunnel sites are connected in parallel before presentation to the respective trunk controllers, as are the even-number tunnel sites.

Internal radio

The Shuttle Internal Radio System is a hand portable to hand portable radio system for use within the EuroTunnel tourist wagons. It can also be accessed from the Train Captain's Control Panel position in each locomotive cab.

The system can be used to provide public address and intercommunications and to act as an emergency telephone. Leaky feeder cable is fitted throughout the train connected by PCM (plug compatible manufacture) links in each wagon and terminated at each end of the train by a repeater base station fitted in the locomotive. This enables the crew to use their hand portable when moving throughout the train.

The portables transmit on a common base receive frequency on one of 20 available CTCSS (continuous tone control squelch system) channels and each end repeater votes its locally received signal against the remote received signal, routed via the through-train PCM link. Each end repeater transmits on one of two base transmit frequencies, and the portables scan on each of the 20 channels between these two frequencies. This is necessary to provide coverage over the length of a full rake (a line of wagons coupled together as one unit) train as the losses in wagon couplers preclude coverage from one end of the train only.

Tourist trains are provided with a VHF FM (88–109 MHz) transmitter and tape system to provide two channels of prerecorded audio, one in English, the other in French, for reception in tourist vehicles. This is known as the On Train Passenger VHF Service. It makes use of the leaky cable system provided for the Shuttle Internal Radio System.

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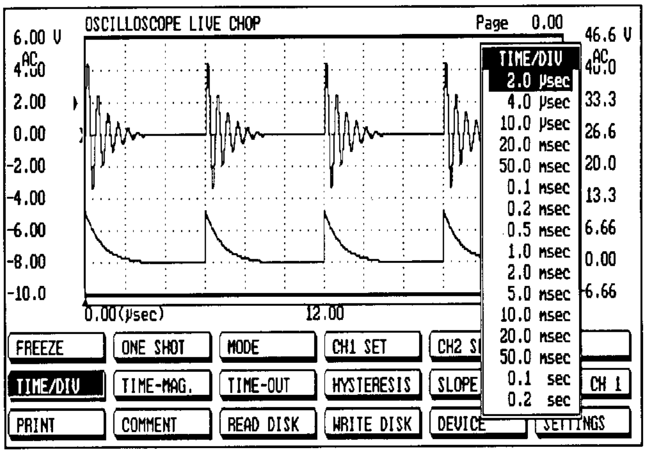
DATA ACQUISITION WITH THE PC



TiePie engineering manufactures a complete range of computer-controlled measuring instruments. Connecting these units to a PC (MS DOS 3.0 or higher) results in a number of comprehensive test instruments:

- oscilloscope;
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- transient recorder.

All measured data can be stored on disk or run off for documentation. Because of the many trigger possibilities, a variety of signals can be measured, while the powerful software enables a multitude of measurements to be carried out in a straightforward manner. Application areas include: service; medical research; automatic test systems; research and development; and education.

LOW COST: HANDYPROBE

Connect the HANDYPROBE to the parallel printer port of the PC and start the software. Measuring can be carried out at once. The HANDYPROBE does not need an external power supply. Some technical parameters: 0.5-400 V software select input range; one input channel; 8 bits resolution (overall accuracy 2%); A complete software program consisting of a digital storage oscilloscope, spectrum analyzer, voltmeter and a transient recorder is provided. The HANDYPROBE is eminently suitable for servicing and educational purposes.

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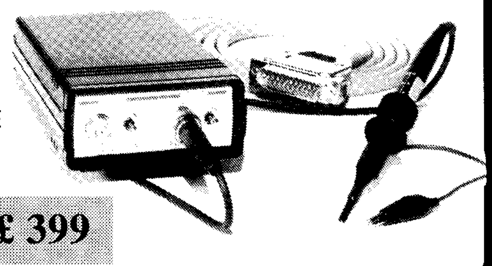
BEST PERFORMANCE: HANDYSCOPE

The HANDYSCOPE is connected to the parallel printer port. This makes it possible to carry out measurements with a laptop or notebook PC. Because of its high resolution (12 bits), the HANDYSCOPE is a very accurate instrument. The measuring rate is 100,000 samples/sec. Either of the two channels can be set independently over a range of 0.5-20 V (with a 1:10 probe up to 200 V). The advanced software enables many measurements to be carried out. Two probes (switchable 1:1-1:10) are provided. The HANDYSCOPE is constructed as a small table model with two BNC connectors. The length of the cable linking the PC and the HANDYSCOPE is 1.8 m, which can be extended to 3.8 m.



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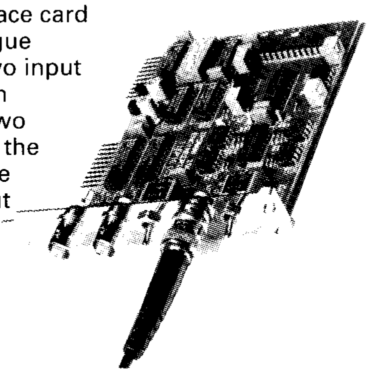
MULTIFUNCTIONAL: TP5008

The TP5008 is an interface card that provides an analogue output in addition to two input channels. This output in combination with the two inputs may be used for the setting up of a complete control loop. The output may also be used as a function generator. The TP5008 has a resolution of 8 bits and a sampling rate of 200,000 samples/sec (200 kHz). The input range may be set to 0.5-20 V full-scale deflection. The output range covers 1.25-2.5 V. The TP5008 is fitted with BNC connectors and is delivered complete with a user manual and software. Separately available are 1:1-1:10 probes and 1:100 oscilloscope probes.



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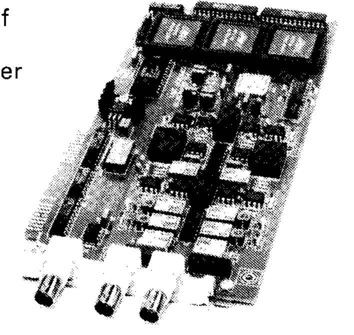
VERY HIGH SPEED: TP208

The TP208 is an interface card with a measuring speed of 2×20 Megasamples/sec (8 bits). Phenomena shorter than one millionth of a second can still be measured well. The completely digitized triggering ensures very stable triggering with many trigger possibilities. The TP208 has an input range of 5 mV/div to 20 V/div in 12 steps and an auto calibration function. Since both channels may be sampled simultaneously, phase differences can be measured very accurately. Even single phenomena can be measured since each channel has a 32 KByte memory. Comprehensive software is provided.



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DOLBY SURROUND

What is it? How does it work?

Based on an article by D. Laues

A description of Dolby Surround must of necessity start with its background, which is in film making. The production of film sound is different from music-studio practice, if only because it evolved separately and, for the most part, earlier. The film industry developed facilities for recording, synchronization amd complex mixes from several sound sources long before the first multi-track sound only reproduction equipment was developed. In fact, many of these techniques antedated the advent of magnetic recording. When filmmakers could not find equipment to implement those techniques, they invented and built it themselves.

One of the most complex systems in the film industry was Cinerama (an early form of widescreen cinematography shot with three adjacent cameras for presentation with three projectors on overlapping panels to form a continuous picture and using seven sound tracks). However, for financial and production reasons, film makers looked for alternative systems.

Involvement of the audience is what films endeavour to achieve and it does not matter whether the means to that end is dramatic or technical. Placing sound sources around the audience has been used universally for almost a decade. But the history of surround sound started with the 35 mm four-track format, which had, however, a narrow and therefore slightly noisy surround track. It was adequate for loud sounds, however, and when it was not in use, a pilot signal on the track shut it off. Fims in 70 mm gave full-width quality on the surround track, making it possible to use subtler sounds and effects.

One of the systems to evolve in the mid 1970s was Dolby Stereo™, which was first used in the film *Star Wars*. In this system, the stereophonic reproduction is extended by a centre channel at the front and a surround channel at the rear of the audience. The centre channel serves to close the gap between the left-hand and right-hand channels; it makes dialogue more intelligible and more natural. The surround channel gives the sound a spatial effect. In cinemas the surround channel is usually reproduced by a number of small loudspeakers that are placed in the form of a U at the back and sides of the theatre. This system is widely used, because it places the information of the four channels on only two tracks of the film, which makes copying simple (which is, of course, important for the film industry). Moreover, it makes Dolby Stereo fully compatible with normal stereo, which means that films made in Dolby Stereo can be run by a standard stereo installation (special effects are, of course, not heard then).

At the time of writing (mid 1994) more than 4000 feature films use Dolby Stereo. Since these films can be viewed at home, either on TV or by video cassette, the Dolby Laboratories introduced, in 1982, a system for consumer applications: Dolby Surround™. This early system was followed in 1987 by Dolby's Pro Logic decoder, which is similar to the professional Dolby Stereo system as far as characteristics and quality are concerned.

How does it work?

A simplified block schematic of a Dolby Stereo encoder, used in the film industry, is shown in **Fig. 1**. It shows how the four channels are combined into two film sound tracks. As far as signals in the centre channel are concerned, this is fairly simple: they are attenuated by 3 dB and then added, in phase, to the left-hand and right-hand channels. The signal in the surround channel is also attenuated by 3 dB and then passed through a bandpass filter, which limits the frequency band to 100 Hz to 7 kHz. It is subsequently applied to a Dolby B compressor and then, phase shifted by –90°, to the right-hand channel, and by +90° to the left-hand channel. The chopping of frequencies below 100 Hz in the surround channel is to protect the surround speakers, which are usually a deal smaller than the front speakers and thus unable to handle these low tones. The limiting to 7 kHz and the compressing provide the required noise reduction. Both measures ensure that any sibilant splatter caused by phase and amplitude errors in the centre channel are reproduced via the surround channel (which would be both unnatural and annoying).

Matrix decoder

A decoder is required to derive the original four channels from the two film sound tracks. This may be an active device (to which will be reverted) or a passive, so-called matrix, decoder. In the latter, the two missing channels are regained mainly by application of sum and difference processes. The basic design of such a decoder is shown in **Fig. 2**. It is seen that the left-hand and right-hand channels are derived directly from the two sound tracks, while the centre channel is formed by adding the two sound tracks together.

The process of obtaining the surround channel is rather more complex. The difference of the two sound tracks is delayed by 20–60 ms, so as to make it impossible for the listener to determine the exact (sound) location of surround speakers close to him. This is essential, because the first wave front must come from ahead, since that must remain the direction of orientation.

Ray Dolby was born in Portland, Oregon, in 1933, and received a B.S. degree in electrical engineering from Stanford University in 1957. From 1949 to 1952, he worked on various audio and instrumentation projects at Ampex Corporation, and from 1952 to 1957 he was mainly responsible for the development of the electronic aspects of the Ampex video tape recording system. After he was awarded a Marshall Scholarship, followed by a National Science Foundation graduate fellowship, he left Ampex in 1957 for further study at Cambridge University in England where he received a Ph.D. degree in physics in 1961, and was elected a fellow of Pembroke College. During his last year at Cambridge, he was also a consultant the the United Kingdom Atomic Energy Authority.

In 1963, he took up a two-year appointment as a United Nations adviser in India, and returned to England in 1965 to establish Dolby Laboratories in London. Since 1976 he has lived in San Francisco, where his company has established further offices and laboratories.

Dr Dolby holds a number of patents and has written papers on video tape recording, long wavelength X-ray analysis, and noise reduction. He is a fellow and past president of the AES (Audio Engineering Society), and a recipient of its Silver Medal Award. He is also a fellow of the British Kinematograph, Sound and Television Society, the SMPTE (Society of Motion Picture and Television Engineers), and a recipient of its Samuel L. Warner Memorial Award and Alexander M. Poniatoff Gold Medal. In 1979 he and his colleagues received the Scientific and Engineering Award of the Academy of Motion Picture Arts and Sciences.

The signal is then passed through a bandpass filter, after which a Dolby expander restores the original dynamics.

The main advantage of a passive decoder is the simplicity of its design. A drawback is, however, that the design does not provide good channel separation. The maximum attainable separation between the four chan-

The Dolby Stereo trademark is used in prints and movie advertisements to denote a Dolby Stereo motion picture and is found only on pre-recorded VHS cassettes that employ B-type decoding on the two standard linear tracks. Furthermore, Dolby Stereo only appears on videocassettes or films that are licensed by Dolby Laboratories. Dolby System may be found on B-encoded cassettes of non-Dolby Stereo films that were released theatrically in four-track magnetic stereo or Academy mono. Therefore, no Dolby logo will be found on a video disc; although the LaserDisc is a high-quality medium, it does not employ Dolby noise reduction. Similarly, while the linear tracks on a VHS cassette might say 'Dolby Stereo', the 'VHS Hi-Fi' logo is not accompanied by any Dolby trademark.

Home surround decoders licensed by Dolby Laboratories have carried the 'Dolby MP Matrix', whose exact meaning was a mystery to most people. To remove this mystery, and to indicate the presence of Dolby Laboratories on the growing number of non-Dolby B home video formats, a new trademark, Dolby Surround, was introduced. The new logo appears on licensed decoders, replacing Dolby MP Matrix, as well as on all forms of video release, including the non-Dolby B stereo formats such as VHS and Beta Hi-Fi. Thus, Dolby Surround indicates the presence of stereo audio with surround information recorded and encoded with a Dolby DS-4.

Obtaining the Dolby Surround logo means that a manufacturer adheres to the basic outline provided by Dolby Laboratories. In general, licensed decoders have to contain:

- Metered input calibration to optimize levels for different VCR and videodisc output levels.
- A basic *L-R* surround matrix to extract the out-of phase surround information.
- A delay line, not only for time coherence of information that is both in the surrounds and front speakers, but also to reduce the perceptibility of unintentional surround leakage, especially the sibilant 'splatter' sometimes caused by azimuth errors. The recommended delay range for home decoders is 10–30 milliseconds (Dolby Cinema Processors are adjustable from 30 to 100 ms because of the larger front-to-back size of motion picture theatres).
- A 7 kHz low-pass filter. This is the high-frequency cut-off chosen by Dolby Laboratories to prevent bothersome hiss coming from surround speakers in theatres during quiet or inactive periods. The relatively steep HF roll-off also helps reduce delay-line noise and rear-channel sibilant splatter.
- A modified Dolby B-type decoder. *L-R* masters contain this modified B-type decoding on the surround-channel information to aid the low-pass filter in noise reduction and masking of sibilant breakthrough. It should be noted that the two tracks on a Dolby Stereo *L-R* always employ A-type noise reduction that is decoded at some stage prior to video cassette duplication. The modified B-type decoding remains on the surround channel.
- An output stage with a ganged master level control.

DOLBY STEREO

DOLBY SURROUND
PRO LOGIC

940059 - 11

Even though dialogue (speech or music) in home stereo playback seems natural coming from the phantom centre, many believe that the addition of a centre speaker helps to lock the dialogue to the image on the television receiver, with benefits observable even on 19-inch (48 cm) sets. In large living rooms, especially, a centre channel can help stabilize the dialogue (which is almost always in the centre) for those seated next to a front (left-hand or right-hand) speaker.

nels is shown in **Fig. 4**.

Pro Logic (active) decoder

Analysis of the output signals of a matrix decoder shows various weaknesses: the two main channels contain information not only from left and right tracks, but also constituents from the centre and surround channels, since these have not been filtered out. Moreover, the surround channel contains constituents from the difference signal, while the centre channel contains parts of both the left and right track.

It is clear that the main task of an active decoder is to improve appreciably the channel separation. This is why it is provided with dynamic direction compensation. The Pro Logic decoder analyses the composition of the signal as far as phase, amplitude and frequency are concerned and generates the necessary correction signals. If, for instance, at a certain instant the left-hand and right-hand signals are identical in amplitude and

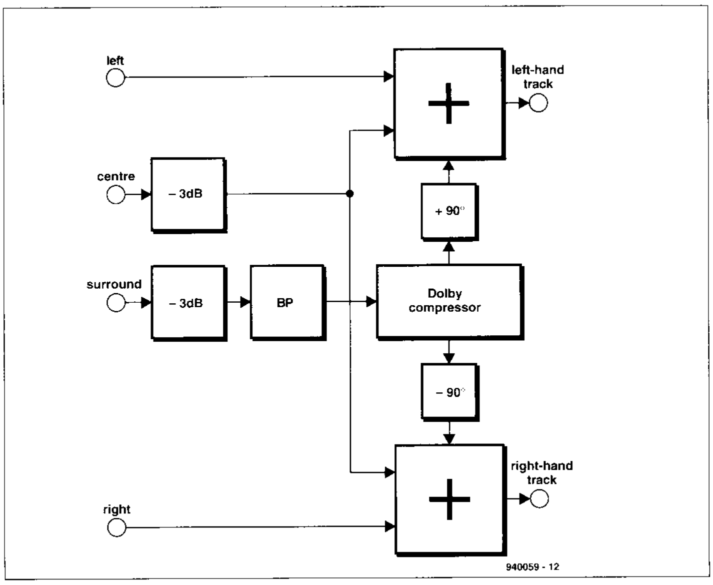

Fig. 1. Simplified block diagram of a Dolby Stereo™ encoder. Note that this is used only in the film industry.

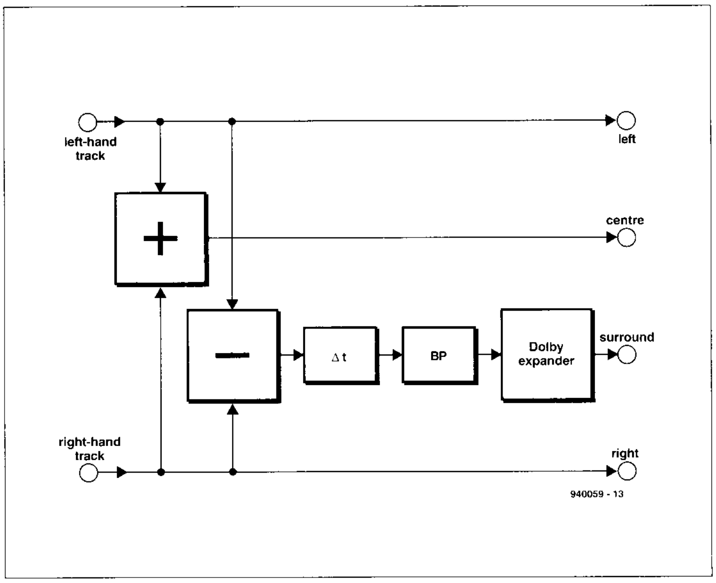

Fig. 2. Block diagram of a Dolby Matrix decoder. Note that this also is for use with film sound tracks only.

phase, the decoder rightly acts as if this mono signal belongs in the centre channel. It then increases the gain of the centre channel and lowers that of the left-hand and right-hand channel to ensure that the total sound volume remains the same.

Active decoders usually have four voltage controlled amplifiers, whose gain is adjusted by the programme material. This selective amplification increases the channel separation between the main and auxiliary channels from 3 dB to 35 dB. Although some perfectionists feel that this is still a low figure, practice has shown that greater channel separation is not necessary, since the four channels form a unified sound source.

The block diagram of the Pro Logic decoder is given in **Fig. 3**. It shows that the basic matrix and preliminary processing of the surround channel signals are identical to those of **Fig. 2**. An addition is the dynamic direction compensation which controls the four voltage-controloled amplifiers (VCAs). In the very latest types of decoder, the entire signal processing and compensation are effected by digital levels. The audio signals are converted into digital levels by an ADC (analogue to digital converter) and processed by a signal processor and suitable algorithms. Filtering and gain control are also by digital levels. The signal delay of the surround channel is effected by DRAMs (dynamic random access memories).

The channel separations obtained with a Pro Logic decoder are shown in **Fig. 5**.

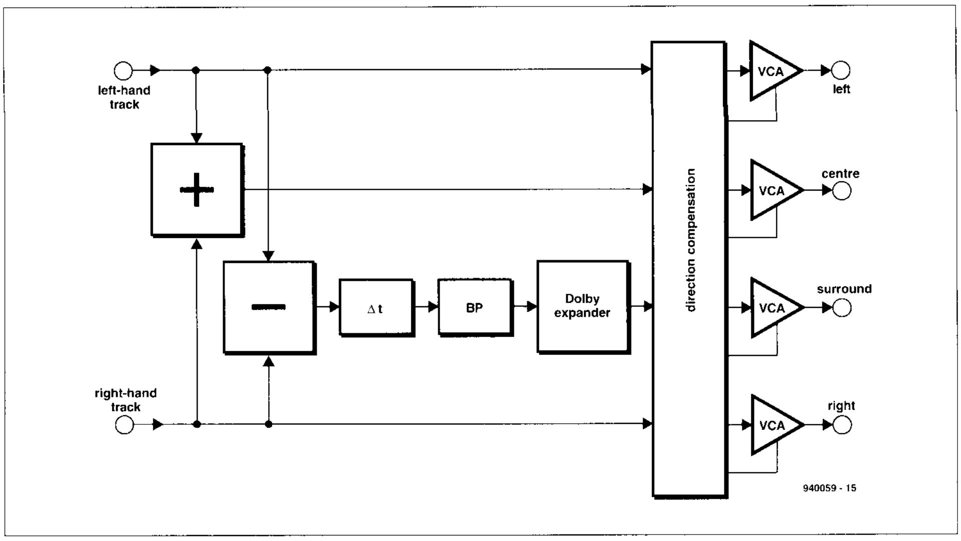

Fig. 3. An active decoder provides dynamic direction compensation, which analyses the signal and continuously adjusts the output levels of the four channels via voltage-controlled amplifiers (VCAs).

Domestic surround

As mentioned before, since Dolby Stereo makes use of only two sound tracks, the sound may be reproduced by any standard stereo installation to which a decoder and an additional pair of loudspeakers have been added. This compatibility with stereo is perhaps the strongest point of the system: it enables the pleasure of listening to surround sound to be removed from the cinema to the living room.

Apart from the fact already mentioned that thousands of feature films have been made in Dolby Stereo, there are many CDs available with original Dolby Stereo film sound tracks (continental Europe: 300+; UK 1000+; USA: thousands). And, of course, many of these film are shown on television. As the TV stations broadcast the original film sound, this can be reproduced in the living room. Consequently, there is a plethora of suitable decoders available from all self-respecting manufacturers: Denon, JVC, Pioneer, Sony, Tshiba, Yamaha, and many others. Prices are coming down, too.

Most of these decoders have a number of additional features. Often there is an integral noise generator which is useful for adjusting the levels of the four channels. An auto balance compensates for differences in output level of the TV. And, of course, there is the inevitable remote control. Some decoders also have provision for connecting a subwoofer: the necessary cross-over filter is already fitted in the decoder. Whether a subwoofer is required depends, of course, on what speakers are already available with the existing audio system.

When buying a decoder or decoder/amplifier for Dolby Surround, make sure that the unit carries the original Dolby logo preceded by the two mirrored Ds and Pro Logic underneath it as shown on the preceding page. Whatever the salesman tells you, equipment that is not so fitted or which carries an incomplete logo is suspect and should not be bought (at least not for the present purpose).

Loudspeakers

A typical loudspeaker array as used in cinemas is shown in **Fig. 6**. To the main speakers for the left-hand and right-hand channel have been added one or more speakers for the centre channel and a series of smaller speakers for the surround channel at the rear and sides of the theatre.

The setup in a domestic living room is rather simpler as shown in **Fig. 7**. Two small speakers for the surround channel and one for the centre channel in addition to the existing stereo speakers are normally sufficient.

There may be some confusion as to what type of loudspeaker should be used for the surround systems. A number of manufacturers offer special sets of speakers and many people will wonder whether there is a need for these. The answer is yes and no. No, emphatically no, as regards the main speakers which should be standard hi-fi units: normally these will be the existing ones. As far as the surround channel is concerned, the usual hi-fi speaker is really too good for this, since the frequency range is limited to 100 Hz to 7 kHz

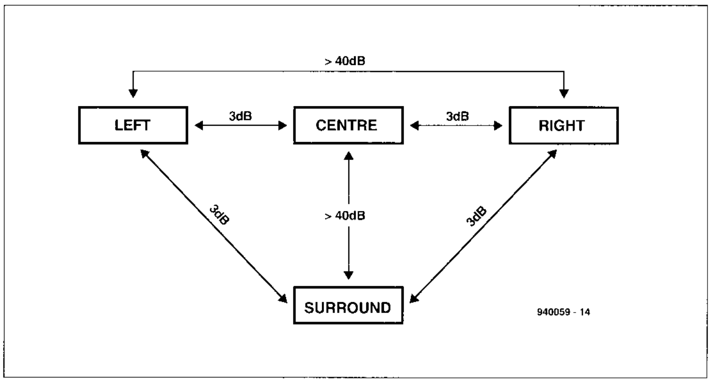

Fig.4. The channel separation provided by a passive decoder is not particularly good.

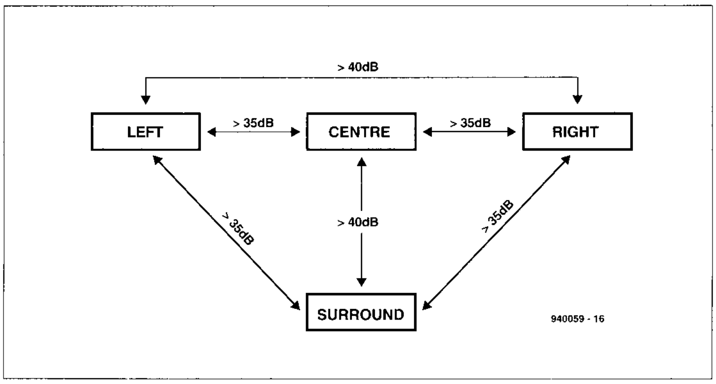

Fig. 5. The control system of an active decoder substantially improves the channel separation.

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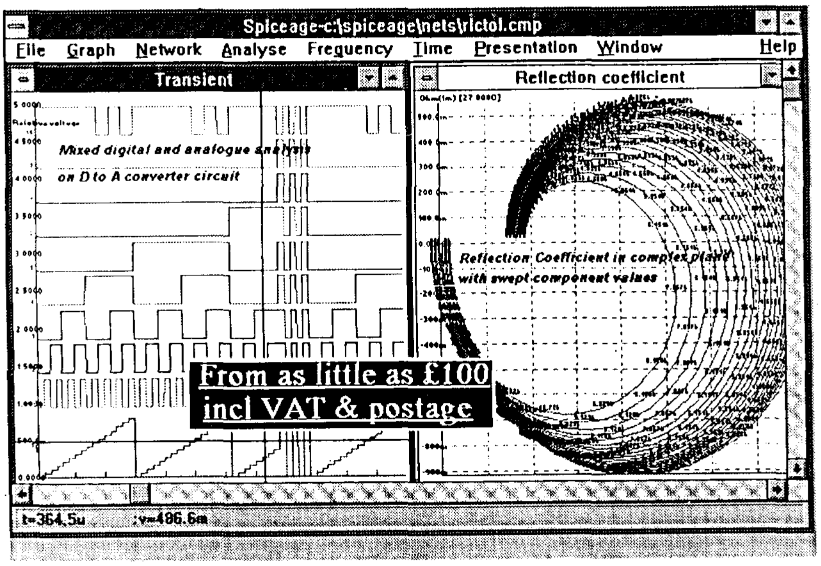
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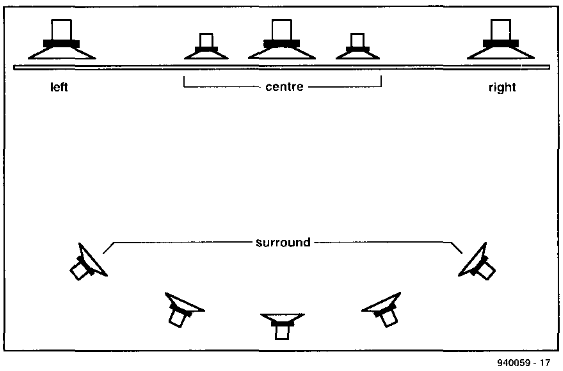

Fig. 6. In a cinema the additional channels are usually reproduced by quite a number of loudspeakers.

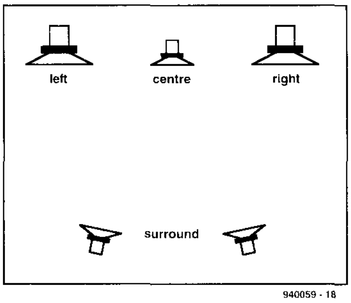

Fig. 7. In a domestic living room, to the existing loudspeakers can be added an additional speaker for the centre channel and two small speakers for the surround channel.

(why use an expensive speaker that goes down to 40 Hz or even 20 Hz?)

The importance of the centre channel must not be underestimated, because this is a real pillar of the Dolby system. Film makers correctly maintain that the centre of the sound of a feature film contains much information, since there virtually all dialogue between actors and actresses take place, as well as much other action. It is at this centre that a standard stereo installation provides no reproduction. Add to this that in most cinemas the left-hand and right-hand speakers are (of necessity) far apart, and it is clear that many viewers find correct localization of the sound impossible.

All this is, of course, not terribly important in the living room, but it illustrates the point that the speaker for the centre channel must be of reasonable quality, although it need not be as large as the main speakers, because it does not handle so much bass power (–3 dB with respect ton the main speakers—see **Fig. 1**). The best pplace for the centre channel speaker is near, but not too close to, the TV set. If too close, the magnet of its drive unit may adversely affect the TV picture. Note, however, that there are speakers available with magnetic screening.

Next month's issue will include a DIY decoder for Dolby Surround.

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74166	1.06
74174	1.37
74175	1.10
74180	1.16
74184	POA
74185	1.76
74191	1.26
74192	1.41
74193	1.65
74221	2.40
74259	2.92
74265	1.46
74273	POA
74276	5.18
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74LS12	0.18
74LS13	0.24
74LS14	0.24
74LS15	0.38
74LS20	0.20
74LS21	0.20
74LS22	0.24
74LS24	0.68
74LS26	0.20
74LS27	0.20
74LS28	0.24
74LS30	0.18
74LS31	1.58
74LS32	0.20
74LS33	0.60
74LS37	0.20
74LS38	0.18
74LS40	0.18
74LS42	0.32
74LS44	2.11
74LS47	0.68
74LS48	0.54
74LS49	POA
74LS51	0.22
74LS54	0.28
74LS55	0.44
74LS73	0.35
74LS73A	0.79
74LS74	0.20
74LS74A	0.26
74LS75	0.25
74LS76	POA
74LS76A	1.05
74LS77	0.44
74LS78	0.32
74LS83	0.39
74LS83A	0.39
74LS85	0.36
74LS86	0.26
74LS90	0.32
74LS91	POA
74LS92	POA
74LS93	0.40
74LS95	0.48
74LS96	0.82
74LS107	0.33
74LS107A	0.78
74LS109	0.33
74LS109A	0.66
74LS112	0.33
74LS112A	0.66
74LS113	0.36
74LS113A	0.42
74LS114	0.36
74LS114A	0.40
74LS122	0.33
74LS123	0.35
74LS125	0.28
74LS125A	0.32
74LS126	0.32
74LS126A	0.40
74LS132	0.29
74LS133	0.35
74LS136	0.78
74LS137	1.58
74LS138	0.34
74LS139	0.42
74LS139A	0.42
74LS145	0.66
74LS147	POA
74LS148	0.87
74LS151	0.35
74LS153	0.36
74LS154	1.23
74LS155	0.38
74LS156	0.38
74LS157	0.42
74LS158	0.38
74LS160	0.52
74LS160A	0.60
74LS161	0.46
74LS161A	0.49
74LS162	1.10
74LS162A	1.10
74LS163	0.40
74LS163A	0.64
74LS164	0.40
74LS165	0.50
74LS166	0.50
74LS168	POA
74LS169	0.50
74LS170	POA
74LS173	0.52
74LS173A	0.52
74LS174	0.33
74LS175	0.33
74LS182	POA
74LS183	POA
74LS189	2.81
74LS190	0.54
74LS191	0.49
74LS192	0.54
74LS193	0.48
74LS194	0.54
74LS194A	0.54
74LS195A	0.56
74LS196	POA
74LS221	0.46
74LS224	10.30
74LS240	0.48
74LS241	0.48
74LS242	POA
74LS243	0.50
74LS244	0.48
74LS245	0.50
74LS247	POA
74LS248	POA
74LS249	POA
74LS251	0.00
74LS253	0.00
74LS256	POA
74LS257	0.00
74LS257A	0.48
74LS258	1.00
74LS258A	0.48
74LS259	POA
74LS260	POA
74LS266	POA
74LS273	POA
74LS275	POA
74LS279	0.35
74LS280	0.86
74LS283	0.45
74LS290	POA
74LS292	14.58
74LS293	0.42
74LS294	14.58
74LS295	POA
74LS295A	POA
74LS298	POA
74LS299	1.76
74LS321	3.29
74LS322	POA
74LS322A	POA
74LS323	POA
74LS347	POA
74LS348	POA
74LS352	POA
74LS353	POA
74LS363	POA
74LS364	POA
74LS365	0.53
74LS365A	0.54
74LS366	POA
74LS366A	POA
74LS367	0.36
74LS367A	0.36
74LS368	0.36
74LS368A	POA
74LS373	0.48
74LS374	0.48
74LS375	0.42
74LS377	0.69
74LS378	POA
74LS379	1.50
74LS381A	POA
74LS385	POA
74LS386	POA
74LS390	0.52
74LS393	0.42
74LS395	POA
74LS395A	POA
74LS396	POA
74LS398	POA
74LS399	0.92
74LS423	0.98
74LS445	POA
74LS450	10.68
74LS461A	POA
74LS465	4.18
74LS467	POA
74LS468	POA
74LS469	POA
74LS490	POA
74LS491A	POA
74LS540	0.80
74LS541	0.80
74LS569	POA
74LS573	1.02
74LS574	1.02
74LS590	5.09
74LS592	5.09
74LS593	7.12
74LS595	5.09
74LS597	5.20
74LS621	POA
74LS622	POA
74LS623	POA
74LS624	2.10
74LS625	POA
74LS626	POA
74LS627	POA
74LS628	1.78
74LS629	2.25
74LS631	POA
74LS639	POA
74LS640	POA
74LS640-1	2.79
74LS641	POA
74LS641-1	2.87
74LS642	POA
74LS642-1	POA
74LS643	POA
74LS644	POA
74LS645	0.68
74LS645-1	2.79
74LS646	4.65
74LS652	POA
74LS669	1.58
74LS670	0.78
74LS673	POA
74LS674	16.89
74LS682	2.62
74LS683	POA
74LS684	3.85
74LS685	POA
74LS686	POA
74LS687	POA
74LS688	1.98
74LS693	POA
74LS794	POA
74LS795	POA
74LS796	POA
74LS797	POA
74LS848	POA
81LS95A	1.25
81LS97A	1.25

74HC SERIES

74HC00	0.22
74HC02	0.22
74HC03	0.28
74HC04	0.22
74HCU04	0.24
74HC05	0.32
74HC07	0.48
74HC08	0.22
74HC09	0.48
74HC10	0.29
74HC11	0.22
74HC14	0.26
74HC14A	0.38
74HC20	0.24
74HC21	0.24
74HC27	0.24
74HC30	0.24
74HC32	0.24
74HC42	0.54
74HC51	0.32
74HC58	0.54
74HC73	0.38
74HC74	0.28
74HC74A	0.28
74HC75	0.48
74HC76	0.48
74HC77	0.52
74HC85	0.52
74HC86	0.30
74HC93	0.48
74HC107	0.48
74HC109	0.46
74HC112	0.50
74HC113	0.54
74HC123	0.42
74HC123A	0.42
74HC125	0.42
74HC126	0.45
74HC131	0.52
74HC132	0.60
74HC133	0.44
74HC137	0.72
74HC138	0.34
74HC139	0.32
74HC141	POA
74HC147	0.68
74HC148	0.72
74HC151	0.40
74HC153	0.42
74HC154	0.62
74HC155	0.72
74HC157	0.42
74HC158	0.54
74HC160	0.74
74HC161	0.42
74HC162	0.74
74HC163	0.42
74HC164	0.42
74HC165	0.55
74HC166	0.88
74HC173	0.76
74HC174	0.42
74HC175	0.36
74HC181	1.94
74HC182	0.59
74HC190	0.88
74HC191	0.68
74HC192	0.78
74HC193	0.76
74HC194	0.78
74HC195	0.78
74HC221	0.58
74HC237	0.76
74HC238	0.64
74HC240	0.46
74HC241	0.78
74HC242	0.98
74HC243	0.98
74HC244	0.48
74HC245	0.48
74HC245A	0.54
74HC251	0.36
74HC253	0.52
74HC257	0.52
74HC258	0.73
74HC259	0.52
74HC266	0.48
74HC273	0.54
74HC279	0.58
74HC280	0.92
74HC283	0.76
74HC294	1.29
74HC298	0.78
74HC299	1.38
74HC323	1.82
74HC352	1.20
74HC353	0.75
74HC354	0.84
74HC356	0.84
74HC365	0.52
74HC366	0.62
74HC367	0.52
74HC368	0.56
74HC373	0.48
74HC374	0.48
74HC375	0.78
74HC377	0.52
74HC386	0.38
74HC390	0.48
74HC393	0.41
74HC423	0.54
74HC521	POA
74HC533	0.98
74HC534	0.98
74HC540	0.69
74HC541	0.69
74HC563	0.88
74HC564	0.88
74HC573	0.68
74HC573A	0.86
74HC574	0.64
74HC589	0.92
74HC590	1.20
74HC592	1.24
74HC593	1.89
74HC595	1.14
74HC597	1.10
74HC620	1.82
74HC623	1.48
74HC633	POA
74HC640	1.36
74HC643	1.36
74HC646	1.88
74HC648	1.88
74HC651	1.49
74HC652	2.40
74HC658	POA
74HC659	POA
74HC664	POA
74HC665	POA
74HC670	1.15
74HC677	POA
74HC678	POA
74HC680	POA
74HC682	POA
74HC684	POA
74HC688	0.74
74HC690	1.62
74HC691	1.82
74HC692	1.82
74HC693	1.82
74HC696	1.82
74HC697	1.82
74HC698	1.82
74HC699	1.82
74HC4002	0.48
74HC4015	1.07
74HC4016	0.58
74HC4017	0.60
74HC4020	0.52
74HC4022	0.74
74HC4024	0.62
74HC4028	0.58
74HC4040	0.48
74HC4046	1.44
74HC4046A	1.90
74HC4049	0.46
74HC4050	0.38
74HC4051	0.74
74HC4052	0.74
74HC4053	0.74
74HC4053A	1.12
74HC4060	0.46
74HC4061	POA
74HC4066	0.50
74HC4066A	0.58
74HC4067	4.72
74HC4072	0.48
74HC4075	0.44
74HC4078	0.46
74HC4094	0.78
74HC4316	0.74
74HC4351	1.05
74HC4352	1.62
74HC4353	1.62
74HC4511	0.84
74HC4514	1.10
74HC4515	1.85
74HC4518	0.87
74HC4520	0.78
74HC4534	POA
74HC4538	0.68
74HC4543	0.98
74HC7001	1.01
74HC7007	0.42
74HC7032	POA
74HC7074	POA
74HC7240	0.98
74HC7241	0.98
74HC7244	0.98
74HC7266	0.66
74HC7292	1.10
74HC7294	1.10
74HC7640	1.98
74HC7643	1.98
74HC7645	1.98
74HC40102	1.32
74HC40103	1.12
74HC40105	1.42

74HCT SERIES

74HCT02	0.24
74HCT03	0.28
74HCT04	0.24
74HCT08	0.24
74HCT10	0.24
74HCT11	0.24
74HCT14	0.28
74HCT20	0.28
74HCT21	0.28
74HCT27	0.28
74HCT30	0.28
74HCT32	0.28
74HCT42	0.48
74HCT73	0.38
74HCT74	0.28
74HCT75	0.38
74HCT85	0.54
74HCT86	0.38
74HCT93	0.60
74HCT107	0.40
74HCT109	0.42
74HCT112	0.42
74HCT123	0.64
74HCT125	0.56
74HCT126	0.54
74HCT132	0.50
74HCT137	0.54
74HCT138	0.32
74HCT139	0.52
74HCT147	0.70
74HCT151	0.52
74HCT153	0.52
74HCT154	1.20
74HCT157	0.45
74HCT158	0.50
74HCT160	0.54
74HCT161	0.54
74HCT162	0.84
74HCT163	0.54
74HCT164	0.52
74HCT165	0.52
74HCT166	0.52
74HCT173	0.52
74HCT174	0.52
74HCT175	0.52
74HCT181	3.24
74HCT182	1.20
74HCT190	0.62
74HCT191	0.59
74HCT192	1.20
74HCT193	0.62
74HCT194	1.20
74HCT195	1.20
74HCT221	0.66
74HCT237	1.20
74HCT238	0.69
74HCT240	0.53
74HCT241	0.58
74HCT242	1.24
74HCT243	1.24
74HCT244	0.54
74HCT245	0.54
74HCT251	1.11
74HCT253	1.11
74HCT257	1.11
74HCT258	1.11
74HCT259	1.24
74HCT273	1.24
74HCT280	1.29
74HCT283	0.64
74HCT297	1.48
74HCT299	1.68
74HCT354	0.74
74HCT356	1.54
74HCT365	1.28
74HCT366	1.34
74HCT367	0.59
74HCT368	1.29
74HCT373	0.52
74HCT374	0.52
74HCT377	0.65
74HCT390	0.68
74HCT393	0.68
74HCT394	POA
74HCT423	0.82
74HCT533	1.63
74HCT534	0.75
74HCT540	0.66
74HCT541	0.74
74HCT563	1.46
74HCT564	1.67
74HCT573	0.74
74HCT574	0.74
74HCT583	1.48
74HCT597	1.52
74HCT640	1.34
74HCT643	1.97
74HCT646	2.40
74HCT648	6.40
74HCT651	POA
74HCT652	POA
74HCT670	1.10
74HCT673	POA
74HCT688	1.10
74HCT4002	0.39
74HCT4015	1.41
74HCT4016	0.52
74HCT4017	0.68
74HCT4020	0.74
74HCT4024	0.68
74HCT4040	0.70
74HCT4046	2.10
74HCT4051	0.96
74HCT4052	0.96
74HCT4053	0.84
74HCT4059	2.24
74HCT4060	0.84
74HCT4066	0.66
74HCT4067	5.78
74HCT4075	0.36
74HCT4094	0.84
74HCT4316	0.68
74HCT4351	1.04
74HCT4510	1.54
74HCT4511	0.94
74HCT4514	1.64
74HCT4515	3.81
74HCT4516	POA
74HCT4520	0.90
74HCT4538	1.02
74HCT7007	0.39
74HCT7038	5.40
74HCT7046	2.80
74HCT40102	2.43
74HCT40103	1.48
74HCT40104	POA

74HC SERIES SURFACE MOUNT

74HC00M	0.32
74HC02M	0.32
74HC03M	0.32
74HC04M	0.32
74HCU04	0.32
74HC08M	0.32
74HC10M	0.32
74HC14M	0.36
74HC20M	0.36
74HC30M	0.36
74HC32M	0.36
74HC74A	0.36
74HC75M	0.34
74HC85WM	0.65
74HC86M	0.36
74HC123AM	0.46
74HC125M	0.46
74HC132M	0.42
74HC138M	0.38
74HC139M	0.38
74HC154WM	0.64
74HC157M	0.38
74HC161M	0.48
74HC164M	0.48
74HC165M	0.57
74HC173M	0.48
74HC174M	0.38
74HC221AM	0.65
74HC240WM	0.55
74HC244WM	0.55
74HC245AW	0.62
74HC251M	0.42
74HC259M	0.69
74HC273WM	0.55
74HC367WM	0.53
74HC373WM	0.55
74HC374WM	0.55
74HC390M	0.57
74HC393M	0.53
74HC540WM	0.76
74HC541WM	0.76
74HC573WM	1.09
74HC574WM	0.84
74HC688WM	0.84
74HC4017M	0.48
74HC4020M	0.48
74HC4040M	0.44
74HC4046M	1.68
74HC4060M	0.48
74HC4066W	0.84
74HC4538M	0.78

74F SERIES

74F00	0.28
74F02	0.28
74F04	0.28
74F06	0.74
74F07	0.74
74F08	0.28
74F10	0.28
74F11	0.28
74F13	POA
74F14	0.36
74F20	0.39
74F27	0.41
74F30	0.28
74F32	0.28
74F37	0.51
74F38	0.44
74F40	0.94
74F51	0.94
74F64	1.24
74F74	0.31
74F85	2.24
74F86	0.34
74F109	0.58
74F112	0.63
74F113	POA
74F114	POA
74F125	0.56
74F126	POA
74F132	0.58
74F138	0.58
74F139	0.58
74F148	POA
74F151	1.47
74F153	0.58
74F157	0.58
74F158	0.80
74F160	0.90
74F160A	POA
74F161	0.88
74F162	POA
74F163	0.88
74F164	0.88
74F166	3.82
74F168	POA
74F169	3.60
74F174	0.80
74F175	0.80
74F181	6.85
74F182	POA
74F189	4.40
74F190	POA
74F191	2.92
74F192	POA
74F193	2.92
74F194	1.36
74F195	2.00
74F219	POA
74F224	POA
74F240	0.60
74F241	0.60
74F244	0.60
74F245	0.66
74F251	POA
74F251A	0.75
74F253	POA
74F257	POA
74F257A	0.56
74F258	POA
74F259	POA
74F260	0.76
74F269	5.54
74F273	0.96
74F280	0.70
74F283	1.00
74F299	POA
74F323	POA
74F350	POA
74F352	POA
74F353	POA
74F365	POA
74F366	POA
74F367	1.42
74F368	POA
74F373	0.60
74F374	0.60
74F377	1.34
74F378	2.72
74F381	5.70
74F385	POA
74F395	POA
74F399	POA
74F412	POA
74F413	POA
74F432	POA
74F521	1.05
74F524	POA
74F533	POA
74F534	POA
74F537	POA
74F538	POA
74F539	POA
74F540	POA
74F541	1.98
74F543	3.57
74F544	POA
74F545	POA
74F547	POA
74F573	2.78
74F574	2.78
74F579	6.59
74F604	5.59
74F620	POA
74F621	POA
74F623	POA
74F646	3.90
74F676	3.22
74F821	POA
74F823	POA
74F825	POA
74F827	3.32
74F841	3.51

74AC SERIES

74AC00	0.38
74AC02	0.49
74AC04	0.40
74AC08	0.40
74AC10	0.40
74AC11	0.40
74AC14	0.40
74AC20	0.40
74AC32	0.40
74AC74	0.48
74AC109	0.64
74AC112	0.81
74AC138	0.65
74AC139	0.65
74AC151	0.68
74AC153	0.65
74AC157	0.81
74AC158	0.65
74AC163	0.80
74AC169	1.98
74AC174	0.65
74AC175	0.80
74AC191	1.38
74AC240	0.92
74AC241	0.92
74AC244	0.92
74AC245	1.10
74AC251	0.60
74AC253	0.60
74AC258	0.60
74AC273	1.10
74AC283	1.40
74AC299	2.06
74AC373	0.94
74AC374	0.92
74AC377	0.98
74AC521	POA
74AC540	0.98
74AC541	0.98
74AC573	1.38
74AC574	1.38
74AC646	POA
74AC648	POA

74C SERIES

74C00	0.50
74C02	0.50
74C08	0.50
74C10	0.50
74C14	POA
74C20	0.50
74C30	0.50
74C32	0.50
74C42	1.78
74C48	1.84
74C73	1.68
74C74	0.89
74C76	1.14
74C85	1.66
74C90	1.16
74C93	1.63
74C150	3.48
74C151	POA
74C154	4.88
74C157	3.02
74C164	1.91
74C221	2.54
74C240	1.38
74C244	1.38
74C373	1.38
74C374	1.38
74C901	0.94
74C902	0.94
74C903	POA
74C906	0.94
74C907	0.94
74C908	1.51
74C911	13.98
74C912	13.98
74C914	0.94
74C915	2.24
74C922	5.60
74C923	6.28
74C925	8.40
74C926	8.40
74C929	POA
80C95	0.76
80C98	0.98

74S SERIES

74S00	0.68
74S02	0.68
74S03	0.78
74S04	0.68
74S08	0.68
74S09	0.68
74S10	1.10
74S11	0.68
74S20	0.68
74S32	0.68
74S38	0.68
74S40	0.25
74S51	0.36
74S64	0.36
74S74	0.83
74S86	0.83
74S112	0.90
74S124	3.13
74S132	1.11
74S133	0.80
74S134	2.15
74S138	0.97
74S139	0.97
74S140	1.02
74S153	1.39
74S157	1.89
74S163	2.79
74S174	1.01
74S175	1.49
74S182	3.62
74S189	2.35
74S195	2.64
74S240	2.31
74S241	2.31
74S244	1.95
74S257	1.34
74S258	1.34
74S260	0.77
74S273	2.68
74S274	2.66
74S280	1.06
74S283	2.09
74S374	2.31
74S394	2.31
74S412	2.31

VOLTAGE REGULATORS

78008AP	1.15
7805	0.44
7805A	0.62
7805FA	0.68
7806	0.68
7808	0.62
7809	0.62
7812	0.44
7812A	0.58
7815	0.48
7818	0.48
7824	0.48
78L05	0.24
78L05A	0.28
78L12	0.24
78L12A	0.28
78L15	0.28
78L24	0.28
78L56	1.10
78M05	0.42
78M05A	0.42
78M12	0.42
78M12A	0.42
78M13A	0.98
78M15	0.42
78S05	0.88
78S12	0.88
78S15	0.88
7905	0.44
7905A	0.54
7905FA	0.68
7909	0.68
7912	0.44
7912A	0.36
7912FA	0.78
7915	0.44
7918	0.44
7924	0.44
79L12A	0.24
79M05	0.42
79M05A	0.52
79M12	0.44
79M12A	0.64
L4805CV	3.40
L4940V5	6.40
LM317MP	0.98
LM317T	0.78
LM338K	4.45
LT1084CT5	6.92
LT1085CT5	6.60
RC4195N	2.40
TL783CKC	6.98

DIODES

1N2986RB	18.20
1N3881	2.54
1N3997A	6.55
1N4001	0.04
1N4002	0.04
1N4003	0.04
1N4006	0.04
1N4007	0.04
1N4148	0.03
1N4149	0.06
1N4150	0.08
1N4446	0.06
1N4728A	0.24
1N4735A	0.24
1N4736A	0.24
1N4740A	0.24
1N4743A	0.24
1N4744A	0.24
1N4756A	0.24
1N5226B	0.09
1N5232B	0.09
1N5234B	0.09
1N5337B	0.48
1N5349B	0.48
1N5352B	0.48
1N5357B	0.48
1N5365B	0.48
1N5366B	0.48
1N5370B	0.48
1N5380B	0.48
1N5401	0.11
1N5402	0.11
1N6287A	1.55
1N825	2.75
1N825A	2.75
1N827	3.14
1SS252	0.20
5082-2800	0.66
5082-2810	1.40
5082-2835	0.44
AA119	0.60
AA144	0.72
AAZ15	0.58
AAZ17	0.58
AAZ18	0.48
BAV10	0.08
BAV45	4.98
BAW62	0.06
BAX16	0.06
BB204	0.32
BB212	2.48
BB405B	0.22
BB809	0.60
BY179	0.42
BY260-200	3.58
BY261-200	3.98
BYV28-100	0.99
BYV32-50	1.60
CV8805	0.60
DS16C	0.40
MV1404	15.90
MV209	1.20
OA200	0.10
OA202	0.20
OA47	0.14
OA90	0.14
P6KE36A	0.88
P6KE47A	0.88
REC53A	0.40
ZPD2.7V	0.06

ZENER DIODES MISC.

BZY93C7V5	6.60
BZY93C15	6.60
BZY93C18R	6.60
BZY93C20	6.60
BZY93C24V	6.60
BZY93C33R	6.60
BZT03C120	0.74
BZX61C9V2	0.09
BZX61C24V	0.09

ZENER DIODES 400mW
2.4V to 75V
Price: 6p each

ZENER DIODES 500mW
2.4V to 200V
Price: 6p each

ZENER DIODES 1.3 WATT
2.7V to 200V
Price:10p each

ZENER DIODES 3.0 WATT
7.5V to 270V
Price:74p each

ZENER DIODES 5.0 WATT
3.3V to 200V
Price:42p each

ZENER DIODES STUD MOUNT 20 WATT
7.5V to 75V
Price: £4.94 ea.

BRIDGE RECTIFIERS

0.9A/200VDIL	0.38
3.0A/200V SIL	0.57
6A/100V SIL	1.60
8A/200V SIL	1.96
35A/100V/Sqr	2.98
KBPC1002	1.64
KBPC3502	2.98
W005-1A/50V	0.32
W02G-1.5A	0.40
2W02	0.40
2KBB10R/SIL	0.66
2KBB20R/SIL	0.70
B80C1500/Sqr	0.35
B80C1500SIL	0.60
SKB6008/60A	POA
SKD6008/60A	POA

CRYSTALS

HC49(HC18/U)

Freq.MHz	
1.843200	1.60
2.000000	1.66
2.453200	9.96
2.457600	1.49
3.276800	0.98
3.579545	1.10
3.686400	1.02
4.000000	1.02
4.096000	1.10
4.194304	1.10
4.433619	1.10
4.608000	1.10
4.915200	1.20
5.000000/S	1.02
5.068800	1.10
5.242880	1.20
5.888200	1.80
6.000000	1.02
6.144000	1.02
6.400000	1.64
6.552000	1.40
6.553600	1.21
7.372800	0.78
8.000000	1.00
8.867230	1.34
9.830400	1.20
10.00000	1.10
10.69500	1.90
11.00000	1.10
12.00000	0.92
13.87500	2.40
14.00000	1.64
14.31818/S	0.85
14.74560/S	1.10
14.74560	1.10
15.00000/S	1.10
16.00000	1.02
16.00000/S	1.20
18.43200/S	1.10
19.66080/S	1.20
20.00000/S	1.60
22.11840/S	1.68
24.00000/S	1.82
27.64800/S	1.20
30.00000/S	6.99
32.00000/S	1.40
48.00000/S	1.68

S = Series

HC33/U

0.204800	8.23
0.307200	6.99
1.000000	3.95
1.843200	3.71
2.000000	4.65
2.097152	3.71
2.457600	1.92
2.500000	1.92
3.000000	2.25

HC49/U4H

3.276800	1.66
3.579545	1.58
5.068800	2.25
7.864320	1.49
8.000000	1.14
10.00000	2.25
11.05920	2.40
12.00000	1.14
14.00000	2.25
16.00000	1.14
20.00000	1.52
24.00000	1.90

UM-1

8.000000	2.25
8.192000	2.02
10.00000	2.25
11.00000	2.25
12.28800	2.66
15.00000	2.25
17.73447	2.80
18.00000	2.50
20.00000	2.25
21.00000	2.25
24.00000	2.80

CRYSTALS MISC.

HC43/T 1.000000	6.99
MINI CYLINDER 0.032768	0.88
WATCH 0.032768	0.82

CRYSTAL OSC. MODULES

8pin DIL Plastic pkg TTL Output
4 Pins spaced at corners of 8pinDIL
Freq.= MHz
4, 4.9152, 8, 10, 12, 16 & 20MHz
Price: £3.66 ea.
24.32.40&50MHz
Price £3.94 ea.

8pin DIL Sealed Metal Package HCMOS Output

13.2mm sq.
Pins spaced at corners of 8pinDIL
Freq.= MHz
3.6864,8,10,12MHz
Price: £4.88 each

16,20,24,32,40&50MHz
Price: £3.84 each

TTL Output 14pin DIL Layout Sealed Metal 4pin Pkg
Freq.= MHz
1MHz **£8.90 ea.**

4,4.9152,6,8,9.8304, 10,12,15,16, 18.432, 19.6608, 20, 24, 25 & 30MHz
Price: £3.52 ea.

32, 32.768, 33.33, 40 & 50, 66MHz
Price: £4.45 ea.

Programmable Crystal Oscillators

EXO-3C SERIES 8pin DIL Plastic Package
Freq.= MHz
12, 14.31818, 16, 16.384,19.6608 & 20MHz
Price: £3.92 ea.

16pin DIL Plastic Package
Programmable for 57 Diff.Frequency

SPG8640AN
0.005 to 600kHz

SPG8640BN
0.0083 to 1MHz

SPG8640CN
0.0064 to 768kHz
BaudRateGenerator

SPG8650BN
0.00083 to 100kHz

PXO-600
0.005 to 600kHz

PXO-1000
0.0083 to 1MHz
All above
Price: £ 9.25 ea.
SPG8651BN
0.00083 to 100kHz
Cal. Tol. 5ppm
Price: £ 10.50 ea.

DC to DC Converters

TDK CE-0344	5.60
3W5R 15-15	27.50
IPL S.010	23.40

1 Watt DC/DC 5V Input ±Output DIL & SIL by Newport
NMA0505±5V
NMA0509±9V
NMA0512±12V
NMA0515±15V
Price: £ 8.85ea.

DC/DC Converters by Computer Products

PM623	24.60
PM671	26.70
PM672	26.70
PM903	44.00
PM951	46.50

RESISTORS

METAL FILM
0.25W 1%
E24 Series
10R to 1M
Pack of 5 = 15p
Pack of 10 = 25p

METAL FILM PRECISION
0.25 WATT 0.1%
E96 Series
100R to 255K
Price: £0.94 each

HIGH PRECISION NON-INDUCTIVE WIRE WOUND
0.15 WATT 0.1%

Temp.Coeff.3ppm
10R,50R,100R,250R, 10K,100K
Price: £3.85 each

HIGH PRECISION NON-INDUCTIVE WIRE WOUND
0.33 WATT 0.1%

Temp.Coeff.3ppm
1R,5R,10R,20R,50R
Price: £3.60 each

100R,120R, 250R, 500R,1K, 2K, 5K, 10K,20K
Price: £3.10 each

MEMORIES

DYNAMIC RAM

4164-10	1.40
4164-12	1.20
4164-15	1.20
41256-8	2.40
41256-10	2.40
41256-12	2.40
41264-15	2.24
41464-12	4.45
41464-10	4.45
4464-10	2.80
414256A-70	3.90
44C256AZ-10	6.95
511000-85	8.45
HM48416AP-15	4.60
HM48416AP-20	4.25
HY53C256LS-80	POA
HY53C464LS-80	POA
HYB511000-85	8.45
KM44C256AZ-10	6.95
M5M4464P-15	4.60
MK4116N-54	2.80
MK4564N-15	1.20
NMC3764N-15	1.60
UPD41464C-12	4.20
UPD41464C-15	4.20
UPD416C-2	3.40
UPD416C-3	3.65
UPD446D-1	2.60

STATIC RAM

2114-3L	3.40
6264LP-10	2.40
6264LP-12	2.40
62256LP-12	4.95
62256LP-10	4.95
CDM6116AE3	5.30
CDM6117AE3	5.85
HM1-6116-5	4.38
HM3-6116-5	3.60
HM6116LP-2	2.60
HM6116LP-3	2.60
HM6117LP-3	5.75
HM62256LP-10	7.93
HM6264ALP-12	3.95
HM6264ASP-20	3.95
HM6267P-35	5.07
HM628128LP-80	18.55
HM66204L-12	15.80
KM62256ALP-10	4.95
LH5164D-10L	2.40
PCD5101P	3.30
UPD43256AGU10L	8.33
UPD43256C-12	5.60
UPD4364C-15	4.70

UVPROMS

27C128-25	3.95
27C64A-15	3.95
27C256-15	3.95
27C256-25	3.95
27C512D-12	6.48
27C1000D-12	8.92
27C4096-12	POA
HM27C101G-20	9.80
HN27C1024HG10	16.63
HN27C64FP-20T	3.40
HN27C64G-15	4.20
HN27C64G-20	4.20
HN462532P	4.50
HN4827128G-25	4.55
HN482764G	3.80
M2716-1F1	3.50
M5L2732K	4.40
M5L2764K	3.30
MBM27C64-20/21V	4.90
MBM27C128-30	4.20
MBM27C256-30	5.10
NMC27C256Q-25	4.95
NMC27C64Q-25	3.66
TMS2516JL-45	4.58
TMS27128JL-25	4.60
TMS2716JL-45	4.60
UPD27256D/21V	5.60
UPD2732A/21V	4.95
UPD27C256D-15	5.80
UPD27C512D-15	6.96
UPD27C64D-25	4.95

EEPROMS

28C64-25	9.80
28C64-15	10.95
28C256-20	18.40
28C256-15	19.60
28C256-15DC	28.50
X2816AD	5.10
X2816AP-25	5.10
X2864AP-35	12.20
24C01	1.62
24C02	2.10
24C04	2.98
24C16	5.40
28C04A-20	4.40
59C11	1.44
93C06	1.12
93C46	1.28
93C56	1.52
93C66	2.16

MISC. MEMORIES

6341-1J	4.58
AM2148-45DC	5.44
AM27S281PC	3.98
IDT7130LA-100P	10.40
IDT7132LA-100P	12.20
MB8414E	4.95
MCM4027AC3	2.80
N82S09N	POA
N82S126AN	2.49
N82S153N	5.80
N82S181AN	6.09
NMC6504J-9	3.40
NMC9306N	1.45
P5101L-1	3.90
TBP18S030N	1.74
TBP24S10N	2.90
TBP24SA10N	3.15
TC5501P	3.50
TC5504AP-2	3.40
TC5517AP-2	4.20
TC5565PL-15	3.60
TMS4014JDL	3.40

RESISTORS SMD
0R0 to 3M3
Case 1206-Pack of 5
Price: £0.30 per pk.

CAPACITORS SURFACE MOUNT

Multilayer Ceramic
63 VOLT
Case Size: 1206
L2xW1.25mm

10pF,22pF,33pF,47pF
100pF,220pF,330pF
470pF,1000pF,2200pf
3300pF,4700pF
10000pF,22000pF
33000pF
Price: 15p each

47000pF 100000pF
Price: 18p each

MICROPROCESSOR & SUPPORT ICs

100114DEC	7.40
100141DC	9.80
6303XP	8.76
6321P	4.20
63485CP32/sm	19.95
63B03XP	10.07
6502	3.76
6502A	3.98
6520P	4.40
6522	4.40
6522A	5.26
6551	4.43
6551A	4.43
65C02P2	5.84
65C02P3	6.98
65C102P2	7.00
65C22P2	4.80
65C51E-1	3.80
65C51E-2	4.38
68000P-8	6.78
68000P-10	7.41
68000P-16	18.20
68000P-8	6.50
68008P-8	7.85
68010P-12	POA
6800P	5.70
6802P	3.90
6803P	7.98
6805E3E	14.75
6810P	POA
6821P	1.90
6840P	3.22
6844P	17.20
6845P	4.86
6845SP	5.40
68A00P	POA
68A09P	4.30
68A21P	1.98
68A40P	2.56
68A50P	2.98
68B09P	3.98
68B21P	1.98
68B40P	2.98
8080A	POA
8085AH-2	5.98
8086	3.40
8086-2	3.90
80C32P	5.95
80C32-16MHz	6.98
80C286-12/pga	48.50
80C286-8/plcc	24.40
80C85A	4.95
80C85A-2	5.94
8118-5CH	7.60
93L34DC	7.08
AM25LS2568P	2.68
AM25LS2569P	2.68
AM2602PC	2.30
AM26LS31DC	2.30
AM26LS31PC	1.26
AM27S191ADC	10.20
AM27S281PC	6.25
AM2964BDC	12.36
AM2965DC	6.36
AM2966PC	3.98
AM29826DC	3.34
AM685DL	9.82
AM8238PC	5.60
AM9050CDC	4.95
AM9050CPC	4.60
AM9102CPC	2.82
AM9114BDM	9.96
AM9551PC	9.66
AM96L02PC	3.35
AY-5-8136	6.45
AY-5-8136-006	6.45
C1164/SMD	4.98
C8231A	59.00
C8253	3.60
CA80C85B	5.98
CD82C85	9.62
CD82C86H-5	9.74
CDP6818AE	8.32
COM8136	6.45
COM81C17	9.41
CP82C54	6.42
CRT-8004-001	9.65
CS8205	8.92
D3232	5.60
D8086	5.48
D8086-2	8.80
D8202A	POA
D8254-2	6.42
D8284A	3.90
D8288	6.48
D82C284-12	9.60
D82C284-8	7.85
D82C288-10	10.96
D82C288-12	11.85
D82C288-8	9.36
D8748H	9.95
DP8228N	6.72
DP8238N	6.72
DP8304BN	2.34
DP8311N	8.51
DS1221	6.44
DS1231-20	4.44
DS1232	3.26
DS3486N	3.20
DS3487N	3.20
DS34C86N	4.98
DS34C87N	4.98
DS3631N	3.92
DS3632N	3.88
DS3633N	3.92
DS3634N	2.81
DS3691N	5.92
DS3862N	16.98
DS5000-32-12	45.40
DS8640N	2.98
DS8820AN	3.45
DS8832N	3.98
DS8836N	2.88
DS8837N	5.72
DS8838N	4.98
DS9636A	1.98
DS9637A	1.68
DS9638A	1.68
DS9639A	1.98
EF6803P	4.68

EF6821P	2.30
EF6850P	2.30
EF68B09P	4.68
EF68B09EP	5.35
EF68B21P	2.55
EP610PC-35	POA
HD1-0165-5	10.96
HD146818AP	4.78
HD3-6402-9	6.16
HD3-6440-9	8.89
HD3-6495-9	8.89
HD44883	POA
HD46505SP	POA
HD46802P	POA
HD6321P	4.20
HD63485PS32	32.50
HD63B03XP	11.95
HD68000-8	11.59
HD6845SP	5.55
HD68A52P	POA
HD68B21P	3.92
HI3-7159-5	20.98
HI3-7159A-5	23.40
HM10422	14.30
ID82C86H	17.06
IM6402AIPL	10.20
IM6402IPL	7.75
IM6403IPL	10.80
IMS2600P-15	4.40
INS8250N	7.80
INS8250N-B	7.80
M5M82C51AP	5.89
M5M82C54P-6	6.57
MAB8031AH12P	4.52
MAB8035HL-6P	5.98
MC10103P	2.89
MC10115L	3.85
MC10115P	2.89
MC146805E2P	8.84
MC68000P12	POA
MC68000P16	18.20
MC68010P10	POA
MC68010P12	POA
MC6802P	2.47
MC6809P	6.78
MC6821P	1.80
MC6840P	5.05
MC6844P	18.40
MC6845P	7.38
MC6850P	3.35
MC68705R3P	25.35
MC68A00P	7.02
MC68A09P	7.62
MC68HC05EOFN	11.96
MC8314P	6.60
MCM6810P	3.00
MCM68A10P	5.35
MM53200N	3.40
MM58167BN	10.64
MM58174AN	14.80
MM58274CN	8.52
MSM5832RS	5.47
MSM80C35RS	4.90
MSM80C39/smd	6.45
MSM80C39RS	7.65
MSM80C85A	3.95
MSM80C85A-2	5.98
MSM80C86	7.60
MSM81C55	4.60
MSM82C51A	3.58
MSM82C53-2	3.98
MSM82C53-5	3.58
MSM82C54-2	4.20
MSM82C55A2RS	5.62
MSM82C59A-2	3.98
MSM82C84A	3.95
MSM82C84A-2	4.38
MSM82C88	12.60
N80C286-10/pl	24.50
N80C286-12/pl	29.54
N80L286-8C2/pl	36.20
N8235N	3.68
N8264N	3.68
N82S126AN	3.25
N82S181F	10.04
NS16450N	4.68
NS16550AFN	12.60
NSC800N-1	10.80
P8032AH	4.45
P8051AH	11.20
P8052AH/Basic	24.99
P8080A	3.90
P8085A-2	5.92
P8085AH-2	6.88
P8088	5.84
P80C31BH	4.54
P80C32/Intel	8.30
P80C51FA	15.94
P80C86AL-2	12.60
P8155H/2	6.98
P8205	2.00
P8212	2.40
P8226	2.40
P8251A	4.60
P8253	4.70
P8255A-5	3.90
P8259	2.85
P8259A	3.20
P8274	15.85
P8279-5	3.20
P8282	2.64
P8286	3.60
P82C54	4.10
P82C54-2	4.80
PAL10L8CN	1.90
PAL12H6CN	1.90
PAL16R4BCN	2.17
PAL20L10CNS	4.35
PAL20X8CNS	3.32
PALC16L8Q-25CQ	POA
PALC20L8Z-45CQS	POA
PALC22V10H-35QS	8.34
PIC16C54RC/P	3.60
PIC16C55RC/P	4.48
PIC16C56RC/P	4.42
PIC16C57RC/P	5.06
PIC16C64-04P	13.98
PIC16C64-20P	23.85
PIC16C64-JW	30.96
PIC16C71-16P	8.94
PIC16C84-10P	12.24
PIC17C42-16JW	35.51

PCD8584P	12.22
PCD8584T	12.22
PCF8566P	8.28
PCF8566T	8.28
PCF8570P	7.85
PCF8573P	6.72
PCF8574P	6.96
PCF8574T	6.96
PCF8591P	11.62
R6502AP	4.82
R6520P	4.40
R6522	4.40
R6522AP	5.80
R65C02P2	6.82
R65C02P3	7.15
R65C02P4	8.95
R65C102P2	6.85
R65C21P2	5.96
R65C22P2	4.80
SAB80C32P	5.95
SAB80C32-16MHz	6.98
SAB8155-P	3.82
SAB8259AP	3.59
SAB80C535-N	11.67
SAB82C54-2-P	4.12
SAB82C55A-2-P	4.80
SC80C451ccn64	13.60
SC87C51CCF40	31.95
SC87C51CCG40	31.95
SCN2661bc1n28	3.35
SCN2661ccn28	3.35
PAL16R4-15CN	2.98
TL16C552FN	12.58
TMP7002NL-2	4.97
TMP8085AP-2	5.98
TMS320C10NL	9.88
TMS320C25FNL	17.20
TMS320C25GBL	67.47
TMS3477NL	6.68
TMS3700NSB	8.78
TMS3702ANS	8.78
TMS3835ANS	7.55
TMS77C01NL	10.74
TMS9900NL	24.40
TMS9901NL	14.16
TMS9902ANL	15.94
TMS9914ANL	23.10
TMS9928ANL	7.40
TMS9995JDL	69.85
UA9636ACP	2.38
UA9637A	2.38
UA9638CP	2.38
UA9639CP	2.38
UM6845B	4.95
UM9151	POA
UM9151-3	POA
UPB8238	POA
UPB8282C	4.98
UPB8284AD	4.98
UPB8286C	4.98
UPD70108C-10	9.10
UPD70108C-8	6.95
UPD70116C-10	12.90
UPD70116C-8	9.20
UPD71055C	4.38
UPD7201AC	11.68
UPD7201C	6.80
UPD765AC	5.42
UPD780C-1	4.76
UPD80C39HC	8.42
UPD8155HD	5.84
UPD8251AFC	4.08
UPD8253C-2	3.98
UPD8253C-5	3.98
UPD8286C	POA
UPD8741AD	12.52
UPD8749HC	13.98
V20-10MHz	9.10
V20-8MHz	6.95
V30-10MHz	12.90
V30-8MHz	9.20
V61C30P	7.80
VC0106N6	8.60
X68HC05EOFN	11.96
Z0800110PSC	16.90
Z0868112PSC	3.20
Z180-MPU	POA
Z8001B-CPU	11.96
Z8018008VSC	8.25
Z80A-CPU	2.52
Z80A-CPU/CMOS	3.97
Z80A-CTC	2.28
Z80A-DART	4.98
Z80A-DMA	3.95
Z80A-PIO	2.44
Z80A-SIO/0	4.48
Z80B-CPU	2.66
Z80B-CPUCMOS	4.66
Z80B-CTC	3.00
Z80B-DART	4.84
Z80B-DMA	POA
Z80B-PIO	2.76
Z80B-SIO	4.60
Z80C00AB6	3.38
Z84C42 CMOS	6.60
Z8681-B1	6.79

TELECOM & SPECIAL FUNCTION ICs

62X0890-U18	3.70
707W02020	5.25
733W00124	5.25
AMA1503GXB	4.68
BAA1505	1.80
CLA25106/plcc	5.95
GA05001GDB	3.20
KR9600P	11.96
KS-49258/plcc	5.92
MJ1454BB	7.65
MK5175N	3.80
OC-147-7	2.40
PBD352303	6.40
PP34C108	6.80
Q4704	3.60
QMV16BP5	7.98
QMV18C	6.95
QMV18CN1	7.85
QMV18CW1	7.85
QMV25C	8.42
QMV62AW1	6.90
S4534-AMI	4.20
SA336931	2.95

SCM66115P	3.40
SGS7P050	4.55
SP1450B	5.76
ULA1RB029E1	6.80
ULA20RK008E	159.72
XR-T5683	3.60
ZNA2L029J-BS	3.80
ZNPCM1J-BS	8.95

LINEAR & MISCS.

3630BM/BB	3.40
49620/BB	POA
555-TIMER	0.20
6341-1J	POA
741-OPAMP	0.18
AD520JN	POA
AD524	21.52
AD534JH	48.27
AD537JH	POA
AD548JN	1.80
AD574AKD	64.66
AD578JN	POA
AD581JH	8.92
AD581KCSA/smd	9.97
AD585AQ	31.56
AD592CN	POA
AD594AD	16.80
AD595AD	15.24
AD648JN	3.40
AD707JN	3.40
AD711JN	2.34
AD712JN	3.72
AD7245JN/KN	POA
AD736JN	9.12
AD741KN	3.69
AD7523KN	9.80
AD7537JN	34.98
AD7537LN	POA
AD7542KN	36.35
AD7543JCWE	POA
AD7578KN	46.15
AD844AN	9.70
ADC0804LCN	6.80
ADC804LCWM	12.10
ADC0820CCN	22.40
ADC0834CCN	10.80
ADC84KG-10	38.98
ADC908HP	18.42
ADDAC80N	POA
ADG201AKN	7.35
ADOP07CN	2.32
AH0015CD	17.20
AY-3-1270	3.60
AY-5-1013	4.60
AY-5-1013A	5.98
AY-5-1250	POA
AY-5-3600-PRO	9.96
BA6109	1.68
BA6208	1.40
CA3046	0.51
CA3046(SMD)	0.89
CA3054	0.94
CA3059	1.20
CA3078AT	2.42
CA3079	0.88
CA3080E	0.70
CA3081	0.96
CA3089E	1.22
CA3094AE	2.16
CA3096AE	3.48
CA3096CE	1.82
CA3097E	2.60
CA3120E	POA
CA3130BT	19.20
CA3130E	1.10
CA3140AE	1.34
CA3140E	0.48
CA3146E	0.90
CA3160E	1.25
CA3240E	1.15
CA3240E1	2.72
CA3260E	1.68
CA3280AE	5.94
CA3280E	3.42
CA555CE	0.20
CA741CE	0.18
CS5503-KD	POA
CX7925B	POA
D169CJ	POA
DAC0800LCN	4.10
DAC0832LCN	10.67
DAC08CP	3.48
DAC08EP	5.06
DAC1008LCN	10.73
DAC1222LCN	20.40
DF1700P	17.91
DG201ABK	3.83
DG211	1.56
DG508ACJ	3.98
DG508CJ	3.25
DS1488N	0.48
DS14C88M/smd	1.65
DS14C88N	1.65
DS14C89AN	1.65
HA12017	1.44
HA13426	11.96
HA17723	1.10
HD75189P	0.80
HEF4754V	22.20
HI1-0201-5	3.95
HI1-508A-5	11.21
HI1-549-5	POA
HI1-574AKD-5	42.50
HI3-0201-5	3.40
HI3-0509A-5	7.15
HI3-201-5	3.20
HIIL1	POA
HS574-AK	18.20
ICL7104-16CPL	26.08
ICL7106CPL	4.87
ICL7107CQH	5.20
ICL7109CPL	9.85
ICL7116CPL	7.84
ICL7117CPL	8.60
ICL7126CPL	8.60
ICL7135CPI	9.95
ICL7136CPL	8.60
ICL7137CPL	8.60
ICL7606CJN	12.24
ICL7611DCPA	1.32
ICL7621DCPA	1.98
ICL7622	POA

ICL7650CPD	5.68
ICL7650SCPD	6.27
ICL7652BCPD	8.24
ICL7652CPD	8.24
ICL7660CPA	1.40
ICL7660SCPA	3.80
ICL7662CPA	4.40
ICL7663BCJA	6.78
ICL7663BCPA	5.10
ICL7664CPA	7.95
ICL7665ACPA	4.98
ICL7673CPA	1.38
ICL8052ACPD	8.73
ICL8068AJD	11.38
ICL8069ccsq	3.75
ICL8069dcsq	2.88
ICL8069DCZR	2.88
ICL8211CPA	2.56
ICL8212CPA	2.48
ICM7170IPG	6.98
ICM7207AIPD	7.94
ICM7207IPD	7.94
ICM7209IPA	4.95
ICM7211Amipl	4.68
ICM7211MIPL	4.68
ICM7212Amipl	4.45
ICM7213IPD	6.98
ICM7216AIJI	29.32
ICM7217AIPI	12.32
ICM7217BIJI	12.98
ICM7217IJI	12.98
ICM7218AIJI	8.68
ICM7218AIPI	8.68
ICM7218DIJI	8.68
ICM7218Eijl	14.76
ICM7224IPL	11.92
ICM7226Aijl	37.20
ICM7226Bipl	32.52
ICM7249IDM	POA
ICM7555IBA	1.20
ICM7555IPA	0.84
ICM7556IPD	1.85
IM6403IPL	12.92
L272	2.74
L272M	2.30
L293B	3.64
L293E	4.82
L297/1	6.98
L298N	7.80
L4805CV	2.89
L487	3.76
L4960	3.76
L702B	3.24
LA6250	POA
LA6358	POA
LA6510	POA
LA6520	POA
LC7132	2.98
LC7522	POA
LC7555	POA
LD111ACJ	POA
LF13508D	18.20
LF311H	10.80
LF347N	2.40
LF351N	0.98
LF353N	0.86
LF355N	1.82
LF356N	1.82
LF357BN	4.98
LF357M/SMD	4.98
LF357N	1.20
LF398N	3.98
LF411CN	1.48
LF412CN	1.98
LF441CN	0.75
LF442CN	0.99
LF444CN	2.71
LH0002CN	18.60
LH0032CG	37.40
LM101AH	6.86
LM10CN	9.24
LM111H	8.60
LM13600N	2.60
LM13700N	2.60
LM1391N	3.40
LM139J	6.60
LM1458N	0.82
LM1496N	2.95
LM1801N	7.92
LM1881N	4.80
LM1889N	7.40
LM1894N	4.16
LM218H	15.75
LM239N	3.90
LM2901N	1.68
LM2903N	1.65
LM2904N	1.42
LM2917N-14	6.10
LM2917N-8	5.80
LM294OCT15	2.95
LM294OCT5	2.50
LM2984CT	7.50
LM301AN	0.36
LM307N	1.39
LM308N	1.65
LM310N	2.98
LM311N	0.64
LM311N-14	2.15
LM312H	8.95
LM317AT	3.48
LM317T	0.70
LM317T-LT	1.60
LM318N	2.98
LM319N	2.84
LM320LZ-12	0.34
LM324AN	3.66
LM324J	2.47
LM324N	0.64
LM325N	9.40
LM3301N	2.60
LM334Z	2.20
LM335Z	2.48
LM336Z-2.5	1.48
LM336Z-5.0	1.48
LM337T	1.15
LM339AN	2.98
LM339N	0.60
LM340AT12	1.98
LM340T-5	0.48
LM340T12	0.48
LM340T15	0.30
LM340T5	0.30

LM343H	8.80
LM346N	3.96
LM348DP	0.40
LM348N	0.40
LM350T	6.85
LM351N	2.60
LM358N	0.32
LM359N	4.68
LM360H	7.72
LM361M/smd	6.40
LM363H-100	16.50
LM369DN	3.82
LM369DRC	3.70
LM380N	1.20
LM381AN	7.88
LM385Z-1.2	2.20
LM385Z-2.5	2.20
LM386M-1	1.65
LM386N-1	1.40
LM386N-3	1.80
LM386N-4	2.60
LM387AN	5.90
LM388N-1	4.25
LM389N	3.40
LM3900N	1.60
LM3909N	2.64
LM3914N	4.40
LM393N	0.30
LM393P	0.30
LM394CN	5.98
LM3999Z	2.76
LM399H	7.85
LM4250J	11.82
LM555CN	0.28
LM565CN	7.48
LM710CH	2.80
LM723CH	2.80
LM723CN	0.70
LM733CN	2.65
LM741CJ-14	2.20
LM741CN	0.45
LM747CH	2.40
LM747CN	0.90
LM78GCP	2.40
LM79GCP	2.40
LM833N	2.82
LS285AB	2.40
LS288B	3.60
LS7210	4.40
LT1006CNB	2.72
LT1010CT	4.58
LT1028CN8	7.32
LT1032CN	4.70
LT1070CT	9.14
LT1083CP	8.82
LT1086CT	2.90
LT1134CN	POA
LTC1052	7.97
LTC1099CN	14.39
LTC485CN8	2.16
LTC490	4.40
M5218AL	POA
M5220	POA
M5238L	POA
M5298P	POA
M706B1	1.25
MAX134CPL	17.95
MAX1232CNG	POA
MAX1232CPA	3.57
MAX1259CPE	POA
MAX162ACNG	POA
MAX232ACPE	4.84
MAX232CPE	2.80
MAX232EWE	3.80
MAX232N	2.80
MAX280CPA	6.94
MAX452CPA	5.38
MAX627CPA	2.98
MAX660CPA	5.72
MAX690ACPA	6.58
MAX693CPE	6.68
MAX694CPA	5.70
MAX697CPE	6.59
MAX7219CNG	7.15
MAX8211CPA	2.28
MAX901BCPE	POA
MC1377P	4.93
MC1413P	0.74
MC14411P	11.38
MC14416L	17.60
MC14495P	4.82
MC145406P	2.10
MC1455P	0.40
MC1455P1	0.60
MC1458P	0.32
MC1488L	2.40
MC1488P	0.38
MC1489AL	2.25
MC1489AN	0.80
MC1489L	2.20
MC1489P	0.48
MC1496N	2.20
MC1558L	3.32
MC1648P	12.40
MC1658P	12.78
MC1709CPI	1.20
MC1723CP	1.20
MC1741CP	0.45
MC3242AP	7.54
MC3301P	0.88
MC3302P	0.60
MC3340P	1.60
MC3357P	3.20
MC3403P	1.40
MC3446AP	6.75
MC3479P	7.92
MC3523U	5.80
MC4024P	12.78
MCT2	0.84
MCT61	1.18
MF10CCN	8.95
ML924	4.90
MM5309N	5.76
MM53105N	4.98
MM80C95N	1.44
MP7570JD	POA
MUX24EQ	9.60
MUX24FP	9.60
MV500DP	3.05
MV601DP	3.36
MV8870DP	7.96
NE5020N	10.84

NE527N	3.71
NE532N	0.60
NE536H	4.90
NE5530N	3.82
NE5532AN	1.58
NE5532N	0.80
NE5534AN	1.80
NE555N	0.20
NE556/SMD	0.70
NE556N	0.38
NE558N	2.28
NE564N	3.42
NE565N	2.94
NE567N	0.65
NE568N	POA
NE570N	4.60
NE571N	3.40
NE589N	4.25
NE592/SMD	1.80
NE592N	1.40
NE592N14	0.92
NE602N/AN	2.98
NE604AN	8.24
NE605N	8.60
NE612AN	2.87
NJ8821DP	12.06
OP07CJ	3.60
OP07CN	0.95
OP07CP	0.95
OP07EP	3.10
OP11GP	5.85
OP177FP	3.71
OP27GP	2.89
OP42FZ	7.44
OP77GP	2.07
OPO7CN	0.95
PCM63P-K	35.80
PM7548HP	18.20
RC4136N	0.98
RC4193N	POA
RC4194N	2.85
RC4207GN	1.92
RC4558	0.90
RC4558P	0.60
REF01CP	3.33
REF01HP	3.33
REF02CP	3.98
REF03GP	3.69
REF25Z	1.12
S2560A	POA
SAA1027	6.51
SAA1043P	7.98
SAA3049P	9.92
SAA5025D	7.65
SAA6002A	10.80
SAS560S	3.40
SED2000FVA	9.60
SFC2301ADC	6.78
SFC2741DC	0.18
SG3524N	4.60
SI7660CJ	1.92
SL1452	6.75
SL2364C	3.97
SL3117B	POA
SL486DP	3.36
SL490DP	2.80
SL560CDP	3.00
SL6270CDP	3.30
SL6700CDP	5.47
SN5281CN	POA
SN55451BJG	2.85
SOC12	0.20
SP1648DG	5.53
SP4534	POA
SP4740DP	4.46
SP8660DP	4.96
STK4141II	5.20
STK5151	POA
STK4171II	7.10
STK4181-V	9.60
STK4192II	7.80
STK4277SL	10.80
TA7215P	7.20
TA7256P	2.60
TA7368P	POA
TA7658P	1.20
TA78005AP	0.48
TA8200AH	POA
TA8410K	2.80
TA8449P	POA
TA8659AN	POA
TAA861A	POA
TBA120S	0.60
TCM1520AP	POA
TCM1531P	POA
TCM1705AN	POA
TCM3105N	9.42
TCM5087N	2.40
TCM5089N	2.40
TDA1023	2.30
TDA1083	2.60
TDA1085A	2.96
TDA1085C	3.80
TDA1151	1.10
TDA1170S	2.80
TDA1515A	4.98
TDA1521A	4.37
TDA1576	3.90
TDA1578A	3.60
TDA2086/A	4.82
TDA2595	3.32
TDA3048N	1.85
TDA3505	POA
TDA3810	POA
TDA440	POA
TDA4510	3.38
TDA4563	3.38
TDA4660	6.60
TDA6579T	POA
TDA7010T	POA
TDA7052	2.52
TDA8702	6.22
TEA1045	POA
TEA1060	4.20
TEA5620	POA
TIPC2801KV	8.40
TL026CP	1.84
TL062CN	0.52
TL062CP	0.52
TL064CD	0.98
TL064CN	0.88
TL064ID/smd	2.10

TL071ACP	1.84
TL071CP	0.64
TL072ACP	1.48
TL072CN	0.50
TL072CP	0.50
TL074ACN	2.85
TL074CN	0.98
TL081CP	0.48
TL082CN/CP	0.81
TL084CN/CP	0.84
TL27L2CD	1.98
TL497ACN	3.44
TL507CP	4.03
TL7702ACP	2.04
TL7705ACP	2.04
TL7705CP	2.04
TL7709ACP	2.04
TL7770-SC	3.82
TL783CKC	5.10
TLC1541IN	16.03
TLC2201CP	3.74
TLC2274CN	2.85
TLC251CP	2.54
TLC2652CP	4.92
TLC2654CP	4.84
TLC271CP	0.84
TLC272CP	1.30
TLC272CD	4.10
TLC274CN	2.40
TLC339CN	1.98
TLC372CP	1.40
TLC551CP	3.68
TLC555CP	0.65
TLC556CN	1.58
TLC7524CN	5.24
TLE2061CP	2.20
TLE2062CP	3.40
TLE2064CN	3.45
TLE2161CP	2.42
TMS3477NL	5.96
TPIC2406NE	7.14
TPIC2802KV	9.42
TPIC6259N	3.28
TPIC6273N	3.28
TPIC6595N	3.28
TSC426CPA	POA
TSC500CPE	POA
TSC7106CPL	6.81
TSC7116CPL	5.80
TSC7126CPL	5.80
TSC7660CPA	1.40
U1096B	4.92
U2066B	2.64
U2400B	5.50
UA2240PC	1.40
UA709CP	0.85
UA709PC	0.85
UA715HC	4.50
UA723CP	0.70
UA733CJ	2.98
UA741MP	0.60
UA741TC	0.28
UA748CP	0.36
UA77000UIC	POA
UA798TC	3.80
UCN5800A	2.40
UCN5801A	2.60
UDN2981A	2.00
UDN2982A	2.00
UDN6118A	1.65
UGN3501M	POA
ULN2001AN	0.44
ULN2002A	0.44
ULN2003AN	0.44
ULN2004AN	1.40
ULN2024A	1.40
ULN2032A	1.40
ULN2803AN	0.84
UM5100	POA
UM5101	3.80
XR2211CP	POA
XTR110KP	9.95
Y1112/TI	4.60
YM3623B	15.48
ZN1034E	3.74
ZN414Z	1.60
ZN415E	1.84
ZN416E	2.74
ZN423	2.20
ZN425E-8	5.97
ZN426E-8	3.68
ZN427E8	12.29
ZN428E-8	6.95
ZN429E-8	2.64
ZN432E	21.49
ZN448E	8.76
ZN449E	4.76
ZNA134E	12.25
ZNA134H	12.73
ZNA234E	16.40

75 SERIES

75107	1.02
75107A	1.02
75108	1.80
75108A	1.84
75108B	2.08
75109A	2.46
75110A	1.36
75113	3.02
75114	3.04
75115	1.60
75116	3.30
75121	2.60
75122	POA
75136	3.10
75138	4.40
75140	2.65
75150	1.60
75150M	2.65
75152	6.36
75154	1.75
75154M	1.75
75155	1.20
75157	4.40
75159	5.45
75160A	5.95
75161A	6.47
75162A	7.59
75172NG	3.68
75173	3.68
75174	3.20

75174NG	3.68
75175	2.60
75176A	1.60
75176B	2.28
75176BT	4.98
75177	2.60
75178	2.60
75182	2.60
75183	2.60
75188	0.40
75189	0.85
75189A	0.85
75361	2.84
75365	2.72
75437A	3.26
75450B	0.64
75451	0.28
75451B	0.48
75452	0.28
75452B	0.48
75453	0.64
75453B	0.64
75454	0.64
75454B	0.98
75462	0.98
75463	1.10
75468	3.60
75469	1.30
75470	POA
75471	1.68
75472	1.48
75473	1.48
75474	2.25
75477	2.10
75491	0.68
75ALS176	2.88
75ALS192	2.88
75ALS193J	3.22
75C1154	2.88
75C1406	2.73
75C185	3.98
75C188	1.20
75C189A	1.32
75C189AD	1.32
75LBC176	2.60

TRANSISTORS THYRISTORS & TRIACS

40406	1.60
40673	2.40
BC107A/B	0.17
BC108A/B/C	0.17
BC109B/C	0.18
BC140-16	0.48
BC146/01	0.58
BC149	0.40
BC157	0.34
BC158	0.34
BC169C	0.14
BC179	0.24
BC182	0.08
BC182A	0.08
BC182B	0.08
BC182L	0.08
BC182LB	0.08
BC183	0.08
BC183C	0.08
BC183L	0.08
BC184	0.08
BC184B	0.08
BC184L	0.08
BC184LC	0.08
BC212-18	0.08
BC212A	0.08
BC212B	0.08
BC212L	0.08
BC212LB	0.08
BC213	0.08
BC213L	0.08
BC214	0.08
BC214L	0.11
BC237	0.08
BC239	0.12
BC307	0.08
BC327	0.08
BC328	0.08
BC337	0.08
BC337-25	0.08
BC489	0.24
BC490	0.30
BC516	0.22
BC517	0.20
BC546	0.05
BC546A	0.05
BC546B	0.05
BC547	0.08
BC547A	0.08
BC547B	0.08
BC547C	0.08
BC548	0.08
BC548B	0.08
BC549	0.08
BC549B	0.08
BC550	0.08
BC550B	0.08
BC550C	0.08
BC556	0.08
BC556A	0.08
BC556B	0.08
BC557	0.08
BC557B	0.08
BC558	0.08
BC558A	0.08
BC558B	0.08
BC559A	0.08
BC559B	0.08
BC560A	0.08
BC560C	0.08
BC184C	0.08
BCY71	0.22
BD131	0.88
BD135	0.44
BD241A	0.98
BD242C	0.52
BD243	0.50
BD516	0.78
BD675	0.52
BD676	0.52
BD679	0.54
BD680	0.56

BD743C	1.90
BDT85	1.12
BDX67B	2.78
BDY96	3.60
BF195-C	0.08
BF199	0.22
BF200	0.16
BF256B	0.38
BF256C	0.38
BF259	0.40
BF324	0.28
BF421	0.12
BF450	0.20
BF451	0.22
BF494	0.16
BF759	0.26
BF961	0.66
BF981	0.90
BF982	0.88
BFG65	1.79
BFR53-2GHz	0.48
BFR91-5GHz	0.90
BFR91A-6GHz	1.20
BFW10	1.20
BFX48	0.49
BFX85	0.59
BFX88	0.30
BFX89	1.59
BFY50	0.34
BFY52	0.34
BFY90	0.92
BS107	0.28
BS170	0.36
BS250	0.52
BSR60	0.48
BSX20	0.38
BSX21	0.48
BSX61	1.85
BT136-600	1.10
BUW46	4.94
BUZ11	1.60
BUZ11A	1.62
BUZ47A	6.90
IRFZ14	1.14
IRFZ20	1.77
J113	0.39
J175	0.68
J270	0.92
JA101	0.48
MBD501	1.10
MJE13070	1.10
MJE340	0.68
MJE350	1.10
MJE520	0.80
MPS3638	0.18
MPSA06	0.12
MPSA13	0.12
MPSA63	0.32
MPSA92	0.24
MPSU05	2.21
MTP8P08	2.80
MTP8P10	2.80
PN3643	0.18
TIC106M	0.78
TICP206D	0.61
TICV106D	0.24
TIP115	0.55
TIP121	0.68
TIP145	1.37
TIP2955	0.88
TIP30	0.48
TIP3055	0.88
TIP31A	0.38
TIP32A	0.40
TIP47	0.80
V275LA10	0.92
VN0104N3	0.92
VN66AFD	1.40
VN90AB	2.96
VP0104-N3	0.92
VP0104N2	0.98
VP0104N3	0.92
ZTX212	0.18
ZTX237	0.26
ZTX300	0.18
ZTX313L	0.28
ZTX320	0.38
ZTX510	0.18
ZTX550	0.24
ZTX551	0.36

TRANSISTORS THYRISTORS & TRIACS

2N2219A	0.28
2N2222	0.28
2N2222A	0.22
2N2369	0.24
2N2369A	0.24
2N2484	0.32
2N2894	0.78
2N2905	0.32
2N2905A	0.32
2N2907	0.30
2N2907A	0.30
2N2923	0.30
2N2243	0.78
2N3053	0.34
2N3055	0.98
2N3441	1.20
2N3553	0.98
2N3684	1.68
2N3702	0.10
2N3704	0.10
2N3706	0.10
2N3725	0.78
2N3789	2.16
2N3819	0.54
2N3866	1.24
2N3904	0.11
2N3905	0.12
2N3906	0.10
2N3958	2.12
2N4037	0.48
2N405	2.30
2N4062	0.32
2N4091	0.78
2N4123	0.10
2N4124	0.20
2N4125	0.18
2N4126	0.32
2N4221A	2.96
2N4236	3.72

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2N4403	0.18
2N4921	1.40
2N5401	0.16
2N5415	0.72
2N5449	0.88
2N5459	0.53
2N5485	0.48
2N5876	1.32
2N6034	0.72
2N6037	0.72
2N6050	3.12
2N6051	3.49
2N6054	2.20
2N6056	1.94
2N6057	2.24
2N6058	2.68
2N6109	0.78
2N6125	2.88
2N6388	0.98
2N6517	0.34
2N6519	0.34
2N6668	1.40
2N696	0.26
2N706A	0.48
2SK129A	5.24
2SK246Y	0.30
3SK45	1.85
3SK88	0.84

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2SA1096R	0.96
2SA1100	0.60
2SA1102	2.10
2SA1104	2.40
2SA1111	0.88
2SA1115	0.20
2SA1145	0.45
2SA1263N	1.80
2SA1264N	2.60
2SA1265N	2.60
2SA1283	0.28
2SA1295	7.32
2SA1302	3.74
2SA1399	0.58
2SA1482	0.78
2SA1515	0.78
2SA1516	3.24
2SA733	0.30
2SA854S	0.52
2SA933	0.24
2SA933S	0.39
2SA965	0.60
2SA968	1.10
2SA970	0.32

2SB1052	1.20
2SB1185	1.52
2SB1238	0.82
2SB750A	1.60
2SB834	1.04
2SB949	1.48
2SB950	1.40
2SC1079	5.80
2SC1115	4.00
2SC1129	0.48
2SC1213	0.40
2SC1279	1.10
2SC1318	0.60
2SC1740S	0.40
2SC1741S	0.32
2SC1775	0.28
2SC1845	0.28
2SC2009	0.44
2SC2180N	8.96
2SC2235	0.40
2SC2238/O	0.76
2SC2238B	0.76
2SC2240	0.24
2SC2275	0.64
2SC2275A	0.88
2SC2278	1.18
2SC2362	0.34
2SC2389	0.36
2SC2497	1.20
2SC2577	1.84
2SC2579	3.20
2SC2591	1.38
2SC2603	0.32
2SC2705	0.44
2SC2928	4.82
2SC3180N	2.38
2SC3181N	2.60
2SC3182N	2.64
2SC3243	0.36
2SC3281	2.72
2SC3284	5.00
2SC3377	0.24
2SC3581	0.56
2SC369	0.44
2SC373	0.44
2SC3907	4.20
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2SC485	1.88
2SC486	1.88
2SC497	1.64
2SC538A	1.98
2SC627	0.68
2SC815	0.68
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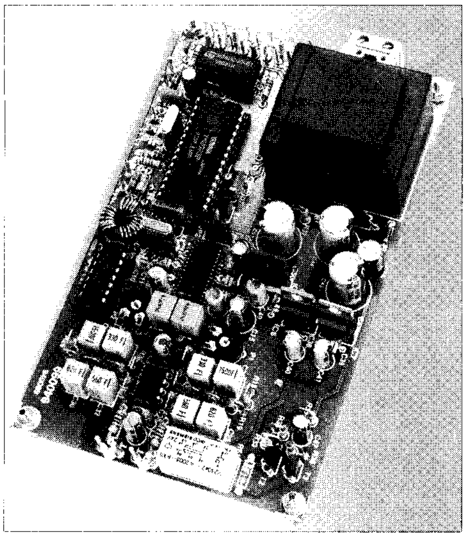
MINI AUDIO DAC

Design by T. Giesberts

A digital-to-analogue converter is described, which is intended to be connected directly to a compact disc player or digital cassette recorder. A special feature of the circuit is the possibility of feeding its clock signal to the digital sound source to prevent the conversion causing any jitter. Including the power supply, it is contained on a printed -circuit board that is somewhat smaller than eurocard size.



Striving for perfect sound reproduction is a way of life for many audio enthusiasts. To that end, this magazine published a digital-to-analogue converter (DAC) in 1992 which had several switched digital outputs. Although the present unit is rather different to the earlier one, it still combines good audio properties with compact construction and reasonable cost.

The converter may be built into an existing compact disc (CD) player, or it can be constructed in a dedicated enclosure for use as a stand-alone unit.

Circuit description

The circuit is dominated by two ICs: interface receiver IC$_2$ and D/A converter IC$_3$.

The S/PDIF input signal is applied via K$_1$ to inverter IC$_{1a}$, which, owing to R$_2$ and R$_3$, operates as a analogue amplifier with a gain of 16 dB. The edges of the output signal of the inverter are enhanced by IC$_{1b}$ and then applied to IC$_2$.

Crystal X$_1$ provides a clock of 16 MHz in the absence of an input signal. Resistor R$_6$ and capacitor C$_6$ constitute the time constant for the internal PLL-VCO (phase-locked loop voltage controlled oscillator). Network R$_5$-C$_5$-D$_1$ resets the clock switching section of the IC when the supply is switched on.

The sampling frequency of the received signal is indicated by D$_2$, D$_3$ and D$_4$. These LEDs are controlled via outputs S$_1$ and S$_2$ of IC$_2$, with IC$_{1c}$ and IC$_{1d}$ functioning as buffers. Output DEF switches on D$_6$ via T$_1$ if the signal has preemphasis.

Diode D$_5$ is an error indicator which is controlled via output ERR. Depending on the nature and type of interference on the input signal, this output is not always active, but often provides short pulses. Network R$_{16}$-C$_9$-D$_7$ enables the circuit to react to these pulses also: it causes the output of the converter to be muted for some tenths of a second when an error occurs. The error signal is buffered by IC$_{1e}$ before it is applied to the mute input of IC$_3$.

A number of signals is applied to IC$_3$ by IC$_2$: the sampling rate clock, LRCIN; the bit clock, BCKIN; the deamphasis switching signal, MD and MC; and, depending on the status of jumper JP$_1$, the oscillator clock, XTI.

The deemphasis must be set according to the three sampling frequencies: in this description it will be assumed to be 44.1 kHz. Note that preemphasis is used only with older CDs. This is just as well, because the internal digital deemphasis is the weak point of IC$_3$: it shows a deviation of almost 1 dB with respect to the theoretical correction characteristic.

The system clock for the converter is provided by IC$_2$ or by X$_2$. This crystal may have a value of $256 \cdot f_s$ or $384 \cdot f_s$, where f_s is the sampling frequency of the applied data. The frequency is set by a logic level applied to pin 23 via jumper JP$_2$.

If a quartz crystal is used, it must also serve as the system clock for the equipment to which the converter is connected. This means, of course, that only one piece of equipment can be connected to the converter, but this will normally not create a problem.

If IC$_3$ derives its clock from IC$_2$, via JP$_1$, the clock frequency is determined by the input signal. This may create a difficulty, however, because the stability of the system clock is all-important for a delta-sigma converter. All jitter and noise are reflected in the audio spectrum and the noise shaping used in this type of converter suppresses these spurious signals only partially. A quartz clock gives much better performance as far as the dynamic range and the signal-to-noise ratio in the audio band are concerned. It is, therefore, advisable to use a separate quartz clock for IC$_3$ and not use the clock derived by IC$_2$ from the received data stream.

This arrangement resembles that of a CD player and stand-alone converter. Such a combination uses two links: one for the digital audio data and the other for interconnecting the system clock between the two units. Although this means an extra link, it is a very good way of obtaining the best from the combination.

The additional output required when the quartz oscillator is used as the system clock for the equipment connected to the converter is provided by IC$_4$ via Tr$_1$ and K$_2$. Since the frequency is 8.192–18.432 MHz, the link between the two units must be 75 Ω coaxial cable.

The transformer prevents an earth loop forming. The specified core material provides excellent coupling so that the theoretical transformation ratio is achieved in practice.

Capacitor C$_{22}$ ensures that the screen of the coaxial cable remains at ground potential. Resistor R$_{10}$ damps any oscillations that may arise in open-circuit conditions, while R$_{11}$ limits any reflections occurring when the cable is not terminated correctly

Main parameters

Sampling frequency: 32 kHz, 44.1 kHz and 48 kHz
Stereo multi-level noise-shaping delta-sigma digital-to-analogue converter
Eight times digital oversampling filter
Integral digital deemphasis
System clock may be connected to CD player or DAT recorder for minimum jitter
Nominal input voltage: 0.5 V into 75 Ω
Nominal output voltage: 2 V r.m.s. ($R_{load} \geq 600\ \Omega$)
Frequency range: 10 Hz to 20 kHz, +0 dB, –0.5 dB
Signal-to-noise ratio: >110 dB, A-weighted
THD+noise at 0 dB and 1 kHz: <0.0025% (measuring bandwidth limited to 30 kHz)
Channel separation: >100 dB at 1 kHz; >75 dB at 20 kHz
Non-linearity: <0.2 dB at signal levels up to –100 dB

to one.

In the connected equipment, the coaxial cable is linked to the input of the IC to which the crystal of the original system clock was connected. It is thus necessary to make sure that the system clock in that equipment is similar to that in the converter. The cable must be terminated by a 75 Ω resistor and connected to the IC input via a 1 nF capacitor. The level at this pin is about 1.5 V_{pp}.

The analogue, third-order lowpass filter in IC_3 gives 0.2 dB attenuation at 20 kHz, which is not sufficient, so that an external filter has been added. This is especially important when 1-bit equipment is used owing to the high noise level present above 20 kHz.

The filter is a fourth-order type based on IC_5, which provides the wanted slope. To ensure equality of the two channels, the

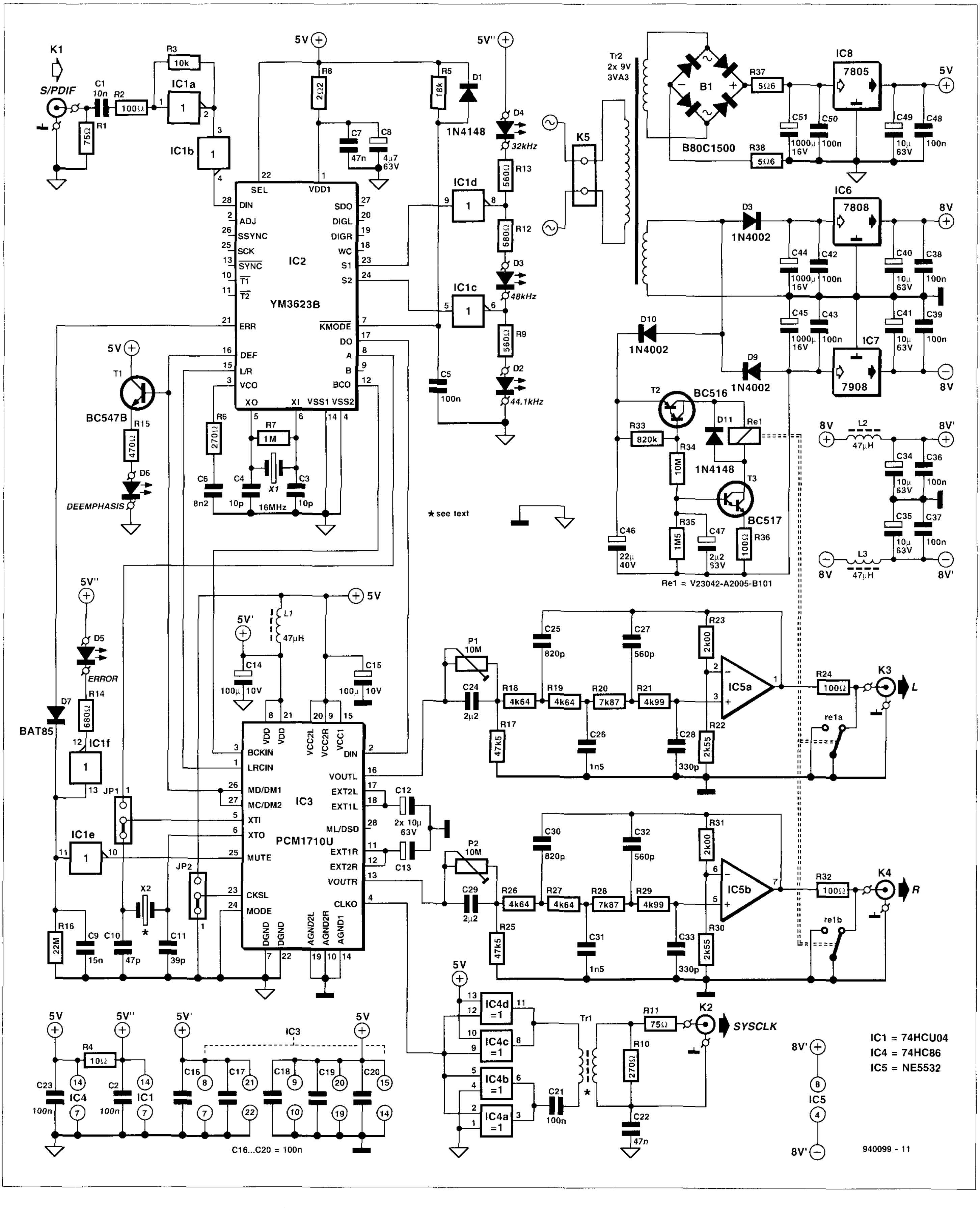


Fig. 1. Circuit diagram of the mini audio digital-to-analogue converter.

The PCM1710U

The PCM1710U from Burr-Brown is a multi-bit, fourth-order delta-sigma digital-to-analogue converter (DAC). The diagram shows the various functions provided by the device. The serial interface accepts 16-bit and 20-bit data formats from most current DSPs or AES/EBU interfaces. As an option, the 16-bit I^2S bus format may be used. To be compatible with systems to come, the device also has a double-speed mode (in which data at twice the current sampling rate of 44.1 kHz can be processed).

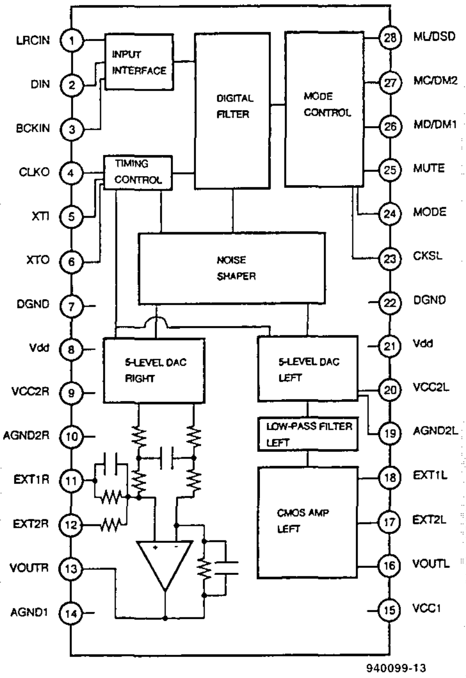
The PM1710U makes an analogue volume control superfluous, because it has an integral, preset logarithmic 127-step attenuator, which may be controlled by a 7-bit code (not used in the present converter, since that would have meant an additional processor). A soft-mute circuit, which prevents spurious signals entering the IC, has been added to the electronic amplitude control.

Before the digital data reach the IC, they are passed through an FIR filter with ×8 oversampling. This gives a damping factor of –62 dB outside the audio band. Here also, if needed, does deemphasis take place at digital level. The ripple in the passband is 0.008 dB.

The basis of the PCM1710U is a newly developed multi-bit delta-sigma converter. The advantage of this over 1-bit converters is the lower oversampling frequency. This results in a more equal distribution of noise over the audio band, which in turn gives a better signal-to-noise ratio at higher frequencies. Moreover, the circuit is much less sensitive to clock-induced jitter. The signal-to-noise ratio is about 100 dB, and the manufacturers specify a dynamic range of 98 dB. Distortion+noise amount to 0.0025%. An additional stage in the IC protects it against externally generated jitter and interference.

The pulse-width-modulated output signal of the IC is reconstructed by an internal passive second-order filter and an active first-order filter. The CMOS op amp used for this delivers up to $3.2\,V_{pp}$ to a load of 5 kΩ.

The PCM1710U, which is housed in a 28-pin SOIC case, requires a single power supply of 5 V.



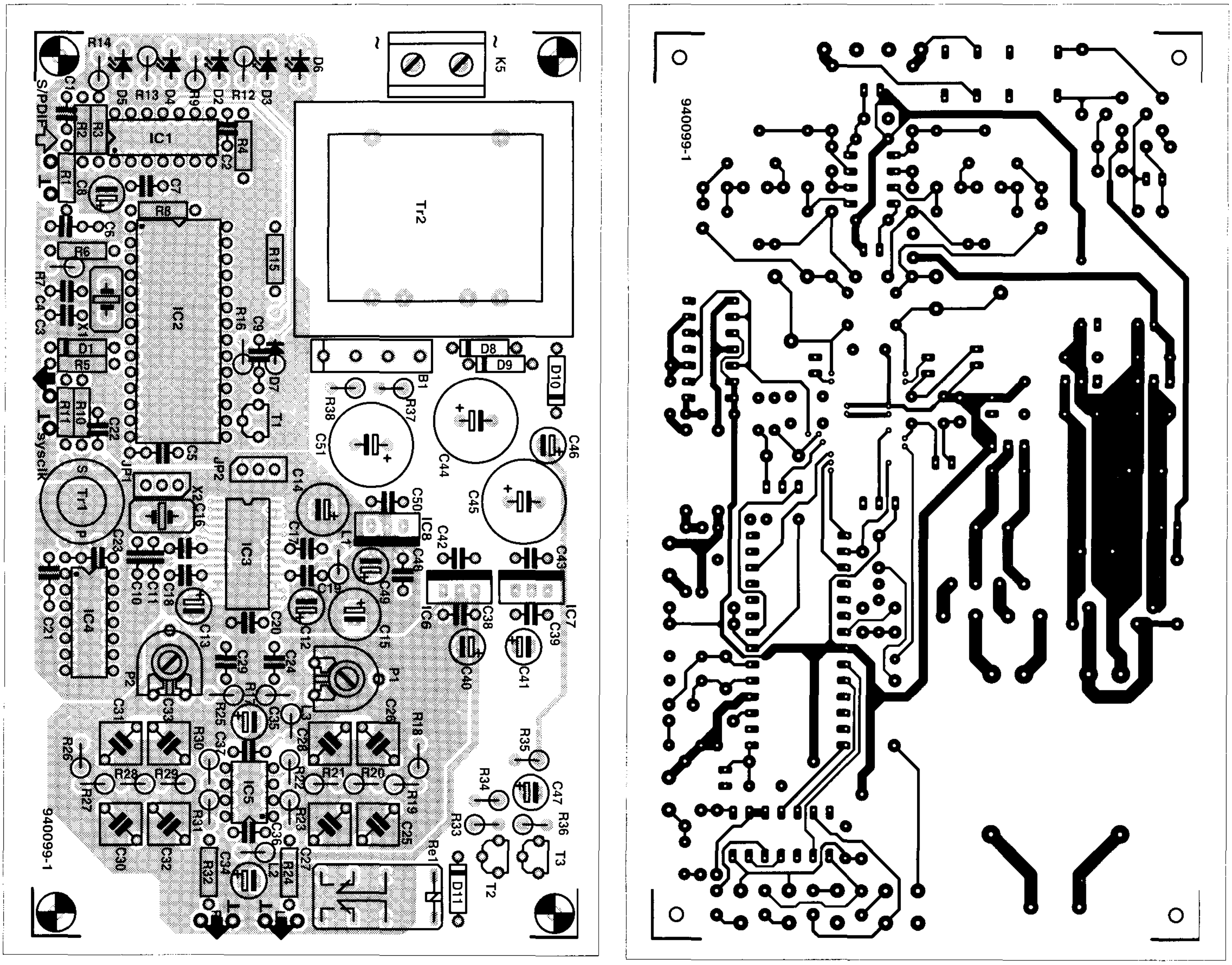


Fig. 2. Printed-circuit board for the D/A converter (overlay on opposite page).

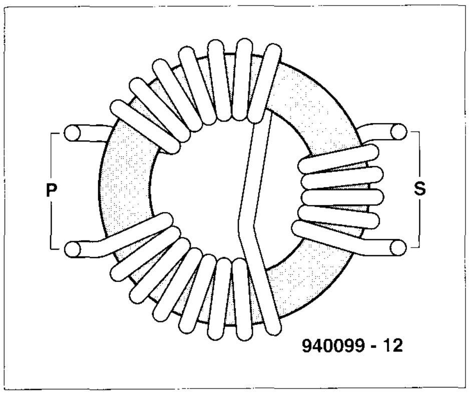


Fig. 3. How to construct the output transformer for the clock signal.

filter components need a tolerance of 1%; Table 1 gives the values for a Butterworth and a Bessel characteristic. The components specified in the parts list have a value that gives a compromise between these characteristics.

The op amps also function as amplifier/buffer. Their gain raises the 3.2 V_{pp} output of IC_3 to 2 V_{rms} at K_3 and K_4. Buffering is needed because the op amp in IC_3 must see a load of ≥5 kΩ. The op amps draw a fairly large bias current, resulting in a rather large voltage drop across R_{17}–R_{21} and R_{25}–R_{29}, which is compensated by presets P_1 and P_2.

Relay Re_1, in conjunction with T_2 and T_3, mutes the clicks caused by on and off switching of the supply. The supply voltage to these transistors, which are cascaded, is 25 V. When the supply is switched on, it takes a few seconds (time constant R_{34}-R_{35}-C_{47}) before T_3 conducts. Resistor R_{36} arranges for T_3 to function as a current source so that the current through the relay has virtually no ripple in spite of the low value of C_{46}.

Transistor T_2 ensures that relay is de-energized rapidly when the supply is switched off, since it will cut off as soon as its base potential, derived from voltage divider R_{33}-R_{34}, drops below 1 V. This value may be altered slightly as required by changing the value of R_{33}.

The circuit uses supply voltages of ±8 V for the analogue section and ±5 V for the digital section. These supplies are isolated from one another up to IC_3 by transformer Tr_2. Resistors R_{37} and R_{38} limit the charging current to C_{51} and decouple the supply lines for RF. The value of C_{51} is higher than usual to reduce the ripple on the supply lines to the digital section to a minimum. The supply line to IC_3 is additionally decoupled for RF by L_1. The supply lines to IC_5 are additionally decoupled for RF by L_2 and L_3.

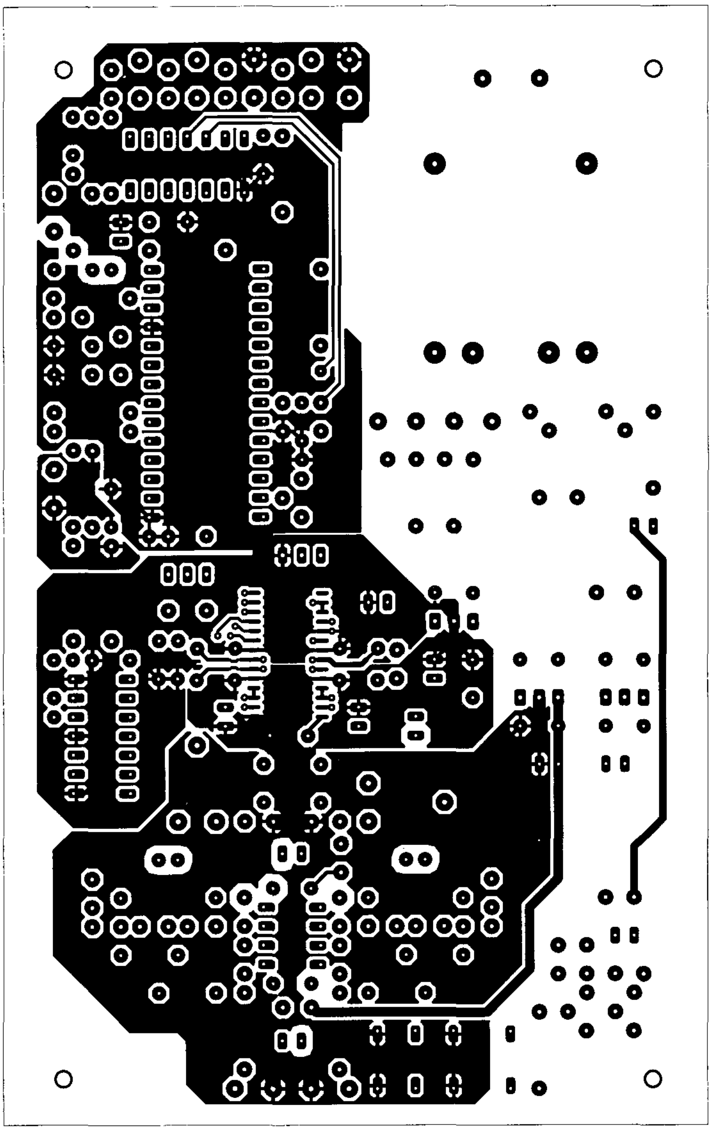
Construction

The converter is intended to be built on the printed-circuit board in **Fig. 2**. Note that a number of components must be soldered in place upright.

If polypropylene instead of polystyrene capacitors are used for C_{25}–C_{28} and C_{30}–C_{33}, the filter characteristic will be slightly less accurate. The capacitors should be matched on a capacitance meter to ensure that their values in the two channels are identical. Deviations between the channels are far more disturbing than a somewhat less accurate filter characteristic. The type of filter is an individual choice. A Bessel type has no overshoot or ringing and the impulse response lacks oscillatory behaviour, but its frequency response is rather less selective than that of a Butterworth type. Also, the latter has good transient characteristics.

Output transformer Tr_1 is formed by laying a 15-turn primary and a 5-turn secondary winding on to a G2-3/FT12 toroidal core as shown in **Fig. 3**. Windings as shown keep capacitive coupling to a minimum. After soldering the terminals in place, fix the transformer on the board with a few drops of appropriate fast-setting glue.

Circuit IC_3 is a surface-mount device (SMD). Such a device is best fixed with a



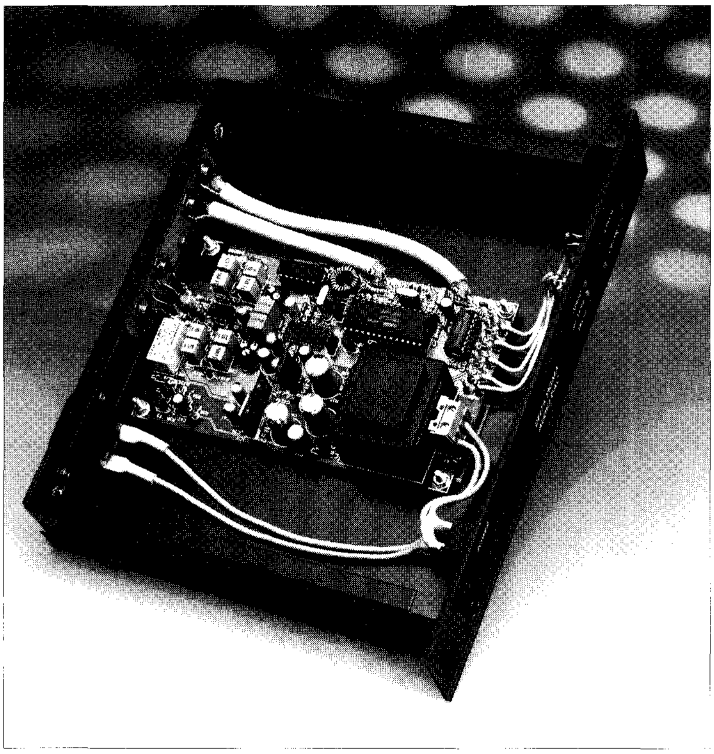


Fig. 4. The D/A converter constructed as a stand-alone unit.

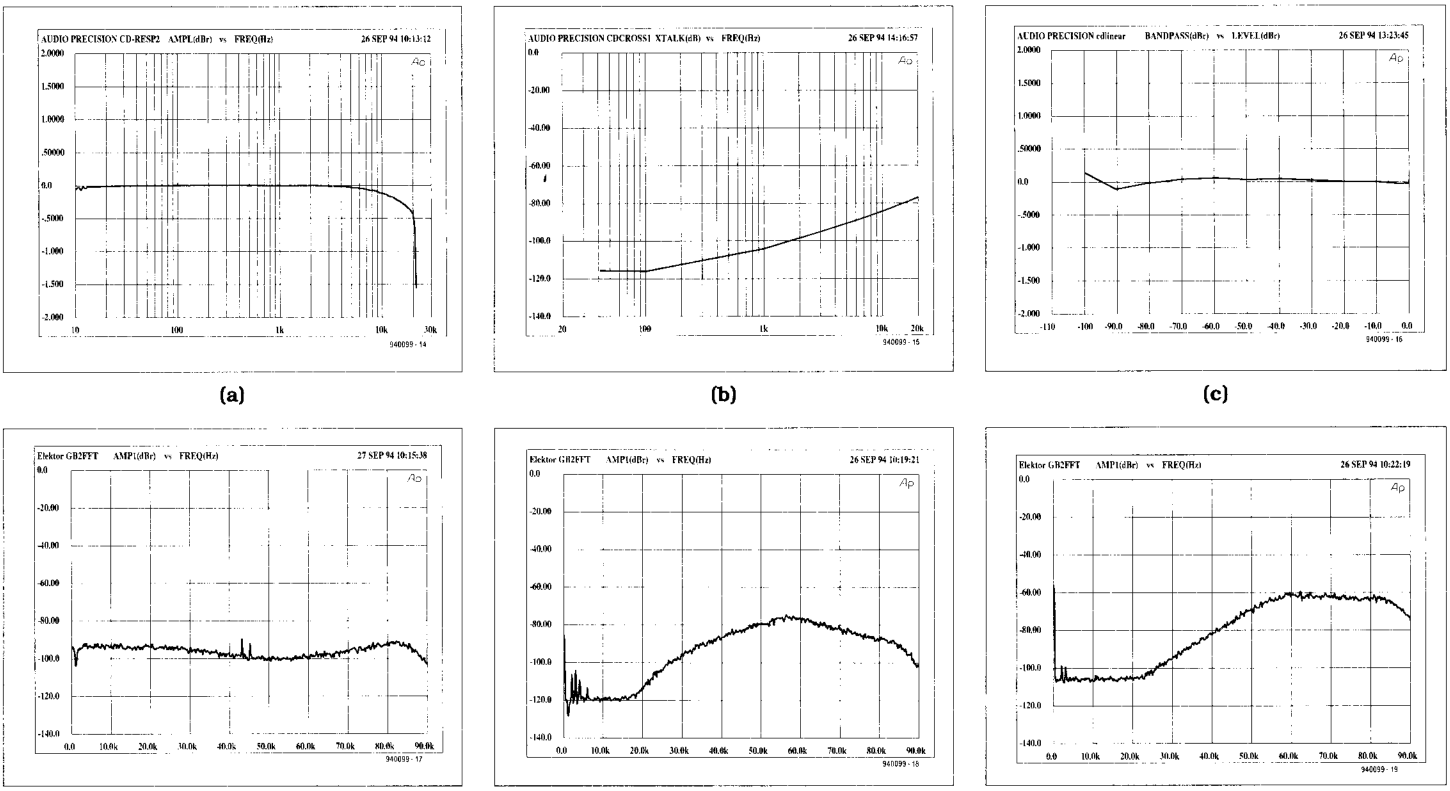
drop of glue: make sure that the pins are in the correct position, and then solder the pins in place.

The answer to the question of whether to use a dedicated crystal for the system clock or not depends on what purpose the converter is to serve. If it is intended to improve the performance of a CD player, open the case of this and note the value of the crystal (modern players use only a single crystal). If the frequency is 11.2896 MHz or 16.9344 MHz, the clock of the converter may be used. In other equipment, such as a DAT recorder (but not a CD player), with a sampling frequency of 48 kHz, the crystal must be 12.228 MHz or 18.432 MHz or, if the sampling frequency is 32 kHz, the crystal should be 8.192 MHz or 12.288 MHz. If so, the clock of the converter may be used. Remove the relevant crystal (and the two customary ceramic capacitors) from the CD player (or DAT recorder) and use it as X_2 in the converter circuit. If the frequency is the lower of the pair stated, set the link of jumper JP_2 between 1 and 2; if the higher of the two, set the link between 2 and 3. Also, set the link of JP_1 between 2 and 3.

The system clock from the converter is connected to the free pins on the relevant IC in the CD player (or recorder). Which way around is quickly seen on the circuit diagram of the equipment. If this is not available, solder the link in place: if the player does not work, reverse the connections.

If the crystals frequencies are different from those given, the converter clock can not be used as the system clock. In that case, omit X_2 and use the system clock of IC_2 by placing the link on JP_1 between 1 and 2. The clock output circuit based on IC_4 and Tr_1 can also be omitted.

Solder pins in the LED positions so that the diodes can be fitted directly on the front panel of the enclosure (if used) and linked to the pins by short lengths of equip-



(a) (b) (c)

(d) (e) (f)

Fig. 5. Measurement results of prototype. (a) The frequency characteristic is virtually straight at 10 Hz, but at 20 kHz the deviation resulting from the output filter is about 0.4 dB. (b) Crosstalk between the two channels. (c) Non-linearity of the converter becomes only noticeable between –90 dB and –100 dB . (d), (e) and (f) are Fourier analyses of a 997 Hz output signal; at (d) the clock for the converter was derived from the digital input signal via the YM3623B; at (e) the converter had a dedicated crystal that was also linked to the CD player; the distortion residue of the 997 Hz signal is clearly visible (THD about 0.001%). The rising of the audio band above 20 kHz is typical of a noise-shaping DAC. The falling off above 50 kHz is caused by the analogue output filter. The noise in the audio band is here almost 30 dB lower than at (d). (f) shows the same situation as in (e), but without the analogue output filter. Note that the noise in the audio band is appreciably higher.

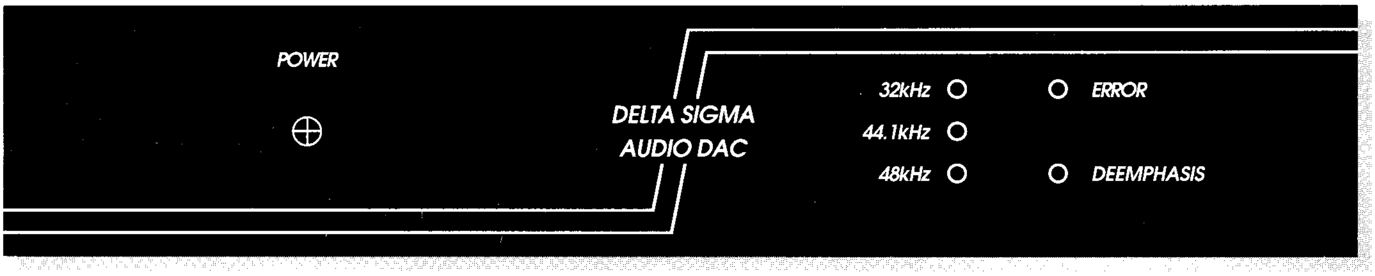


Fig. 6. Suggested front panel for the D/A converter (not available ready made) (scale 3:4).

Butterworth
Attenuation at 20 kHz (filter + DAC): about 0.3 dB
R_{18}, R_{20}, R_{26}, R_{28} = 10.7 kΩ, 1%
R_{19}, R_{27} = 3.65 kΩ, 1%
R_{21}, R_{29} = 3.16 kΩ, 1%
C_{25}, C_{30} = 1 nF, 1%
C_{26}, C_{31} = 1.5 nF, 1%
C_{27}, C_{32} = 560 pF, 1%
C_{28}, C_{33} = 330 pF, 1%

Bessel
Attenuation at 20 kHz (filter + DAC): about 1 dB
R_{18}, R_{26} = 6.49 kΩ, 1%
R_{19}, R_{27} = 2.87 kΩ, 1%
R_{20}, R_{28} = 5.49 kΩ, 1%
R_{21}, R_{29} = 2.49 kΩ, 1%
C_{25}, C_{30} = 820 pF, 1%
C_{26}, C_{31} = 1.5 nF, 1%
C_{27}, C_{32} = 560 pF, 1%
C_{28}, C_{33} = 330 pF, 1%

Table 1. Component values for different types of filter.

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ment wire. The LEDs are not required if a common system clock is used.

The board may be built into a CD player or constructed as a stand-alone unit (see **Fig. 4**). If the latter, a suggested front panel layout is shown in **Fig. 6**. Make sure that the audio output sockets at the rear of the enclosure are in line with the relevant connections on the board. Also, sockets are required for the system clock (if used) and the digital audio signal. These must be connected to the board by short lengths of coaxial cable. Finally, a mains entry with integral fuse and a mains on/off switch must be fitted

Adjusting the presets

Connect a multimeter (set to lowest direct voltage range) to one of the the outputs of the converter. Switch on the mains and let the circuit warm up for 10–15 minutes. Do not apply an input signal and adjust the relevant preset for zero reading. Connect the multimeter to the other output and adjust the other preset for zero reading.

Parts list

Resistors:
R_1, R_{11} = 75 Ω
R_2, R_{24}, R_{32}, R_{36} = 100 Ω
R_3 = 10 kΩ
R_4 = 10 Ω
R_5 = 18 kΩ
R_6, R_{10} = 270 Ω
R_7 = 1 MΩ
R_8 = 2.2 Ω
R_9, R_{13} = 560 Ω
R_{12}, R_{14} = 680 Ω
R_{15} = 470 Ω
R_{16} = 22 MΩ
R_{17}, R_{25} = 47.5 kΩ, 1%
R_{18}, R_{19}, R_{26}, R_{27} = 4.64 kΩ, 1%
R_{20}, R_{28} = 7.87 kΩ, 1%
R_{21}, R_{29} = 4.99 kΩ, 1%
R_{22}, R_{30} = 2.55 kΩ, 1%
R_{23}, R_{31} = 2.00 kΩ, 1%
R_{33} = 820 kΩ
R_{34} = 10 MΩ
R_{35} = 1.5 MΩ
R_{37}, R_{38} = 5.6 Ω
P_1, P_2 = 10 MΩ preset

Capacitors:
C_1 = 10 nF ceramic
C_2, C_{16}–C_{21}, C_{23}, C_{36}–C_{39}, C_{42}, C_{43}, C_{48}, C_{50} = 100 nF, ceramic
C_3, C_4 = 10 pF
C_5 = 100 nF
C_6 = 8.2 nF
C_7, C_{22} = 47 nF ceramic
C_8 = 4.7 μF, 63 V, radial
C_9 = 15 nF
C_{10} = 47 pF
C_{11} = 39 pF
C_{12}, C_{13}, C_{34}, C_{35}, C_{40}, C_{41}, C_{49} = 10 μF, 63 V, radial
C_{14}, C_{15} = 100 μF, 10 V, radial
C_{24}, C_{29} = 2.2 μF, polypropylene, pitch 5 mm
C_{25}, C_{30} = 820 pF, 1%*
C_{26}, C_{31} = 1.5 nF, 1%*
C_{27}, C_{32} = 560 pF, 1%*
C_{28}, C_{33} = 330 pF, 1%*
C_{44}, C_{45}, C_{51} = 1000 μF, 16 V, radial
C_{46} = 22 μF, 40 V, radial
C_{47} = 2.2 μF, 63 V, radial
*polystyrene (preferred) or polypropylene

Inductors:
L_1–L_3 = 47 μH

Semiconductors:
D_1, D_{11} = 1N4148
D_2, D_6 = LED, yellow, low current
D_3, D_5 = LED, red, low current
D_4 = LED, green, low current
D_7 = BAT85
D_8–D_{10} = 1N4002
B_1 = B80C1500 rectifier bridge
T_1 = BC547B
T_2 = BC516
T_3 = BC517

Integrated circuits:
IC_1 = 74HCU04
IC_2 = YM3623B (Yamaha)
IC_3 = PCM1710U (Burr-Brown)
IC_4 = 74HC86
IC_5 = NE5532
IC_6 = 7808
IC_7 = 7908
IC_8 = 7805

Miscellaneous:
JP_1, JP_2 = 3-way PCB header with link
K_1–K_4 = audio socket (chassis mounting)
K_5 = 2-way terminal block, pitch 7.5 mm
Core for Tr_1 = G2-3/FT12
Enamelled copper wire 0.7 mm dia. (for winding Tr_1) as required
Tr_2 = mains transformer, 2×9 V, 3.3 A
X_1 = crystal, 16 MHz
X_2 = crystal 11.2896 MHz or 16.9344 MHz
Re_1 = relay with 2 change-over contacts, coil 12 V, 10 mA
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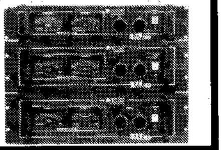

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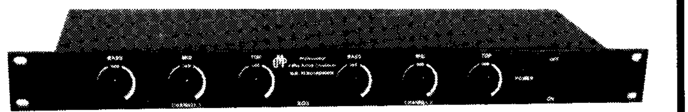

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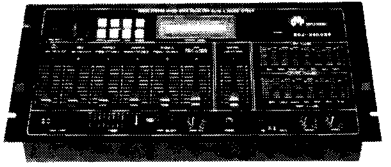

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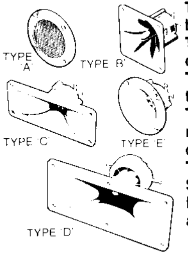

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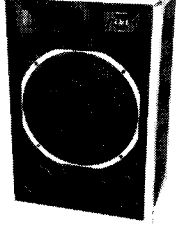

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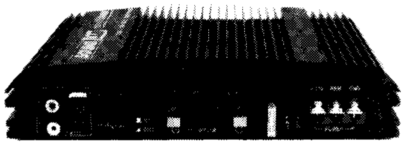

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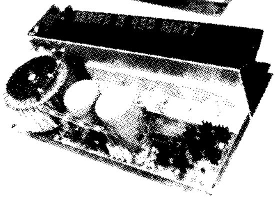

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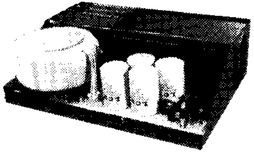

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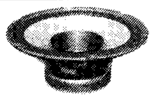

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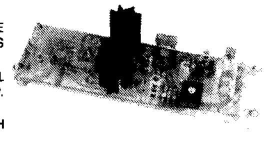

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DEBUGGING 8031/8051 MICROCONTROLLER SYSTEMS

Getting a microcontroller system to function properly is no mean task, not even for the truly initiated. Such systems typically look dead as a doornail even if the slightest malfunction exists. The hardware and software described in this article enables recalcitrant 8051/8031 based systems to be scrutinized in great detail using only a PC and a simple test adaptor.

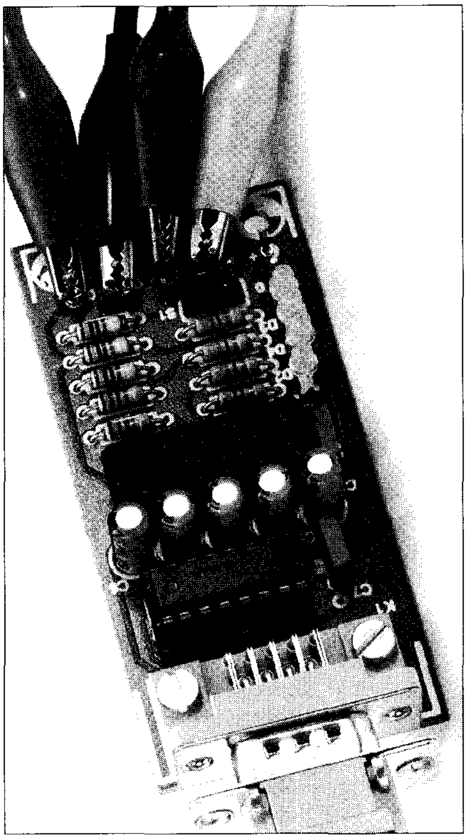
Hardware and software by Dr. M. Ohsmann

THE measurement adaptor proposed here will cost you not more than a fiver for the hardware. Together with the 'Analystor' (for 'analyser/storage') software distributed via the *Elektor Electronics* Readers Services, the adaptor functions as a kind of digital oscilloscope or logic analyser, and is suitable for many purposes.

The test system allows many signals and their relations to be examined in that crucial phase immediately after the reset pulse. The concept is also useful for testing other clock controlled systems. Bus contention and other problems can be analysed with the aid of timing diagrams written by the test program in the form of files. These files are useful for study, reference and analysis.

In nearly all cases, a microcontroller system comprises a CPU (central processing unit) and a program memory in the form of EPROM. If, for instance, the 80C32/8051 single-board computer described in Ref. 1 is built and fitted with an EMON51 EPROM (Ref. 2), it is safe to assume that the hardware design and the software are all right. However, if nothing works when the system is switched on, many users find themselves hopelessly lost for assistance. An even more complex situation arises if you do not know if the program in EPROM is correct, or if the hardware is an experimental design which is being powered up for the first time. Very few designs work first time!

Many of you will be able to avow that the strangest things happen without any apparent logic, as long as there is a single connection error or bus short-circuit anywhere in a microcontroller system. In such cases, one is often desperate for reassurance that the processor properly executes the first few instructions after a reset. That, unfortunately, is not as simple as it looks. The reset pulse is often pretty long, (several hundred milliseconds), and is a bit difficult to time accurately when generated by an *RC* network. Once the processor starts, things appear to happen at lightning speed: an 8051 running at a 12-MHz clock, for instance, executes at least five instructions in the first 10 µs after the reset. To be able to examine what is going on at such high speeds requires either very expensive test equipment, or a bright idea. The main problem is, obviously, the speed. So, why not reduce the clock speed, and make a 'slow motion' recording of what is going on in the system? The PC can be exploited for this purpose, i.e, it can be used to generate the slow clock as well as the reset signal for the microcontroller system under test. After the reset, the processor is clocked so slowly that it becomes possible for the PC to read and display a set of essential signals. In fact, the software supplied for this project displays up to 17 signals on the computer screen, allowing you to monitor, for instance, all databus or address bus activity. The timing diagram is triggered appropriately by the PC itself, so that all memory read/write operations become visible. In short, the PC stretches the time scale during which otherwise almost elusive signals occur.



Using a very slow clock requires the processor to have a so-called static structure. Actually, the inspiration to develop the present debugging system came from the news that a static version of the 8051, the AT89C51 from Atmel, is now available. Apart from being capable of fully static operation (i.e., clock speed actually down to 0 Hz) this new processor, another derivative of the 'generic' 8051, also boasts four EEPROM memories. Actually, the above concept functions properly only with the AT89C51, because a normal 8051 has a minimum clock frequency of about 3.5 MHz. In practice, however, a large number of processors do allow quasi-static operation, although that is not specified by the manufacturer. Among the MCS-51 derivates successfully used in this respect are:

Atmel AT89C51 (fully static)
AMD P80C31BH
MHS P-80C32
Signetics SC87C51CCN40
Philips 80C51BH-3
Siemens 80C535

Obviously, the concept proposed here can be transferred to other processor types, or, indeed, any other logic system capable of static operation, of which the behaviour during the first few hundred microseconds after the reset pulse is to be examined for the purpose of fault-finding. Interestingly, the software for the test adaptor is written in Turbo-Pascal 5.0, and the relevant source files are supplied on disk along with the executable program. Modifications to meet individual requirements are, therefore, relatively simple to make.

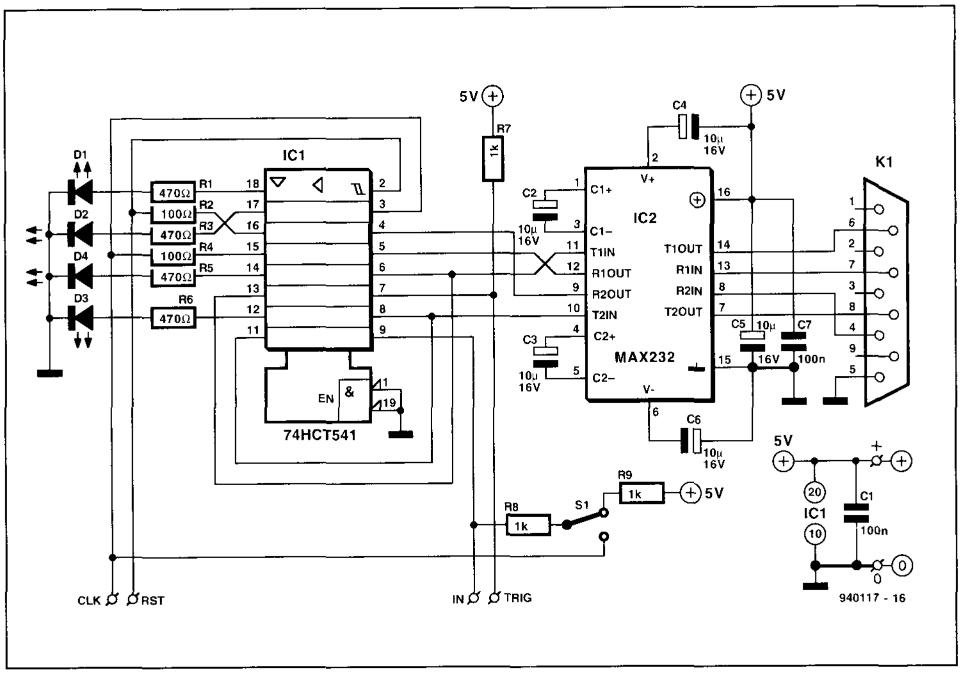


Fig. 1. This simple test adaptor, plus a clever program running on a PC, allows every step, however fast and misguided, of an 8051-type microcontroller to be traced.

The measurement adaptor

The measurement adaptor, whose circuit diagram is given in **Fig. 1**, is connected to the PC via the RS232 interface. As already mentioned, the PC generates the reset and clock signals for the system under examination. This is achieved by using the RTS and DTS handshake lines available on the PC's RS232 port. Two more handshake lines, DSR and CTS, are used to read signals from the system into the PC. The conversion to TTL level is accomplished by the cheap and generally available MAX232 integrated circuit. Next comes a 74HCT541 which functions as a buffer and LED driver. All four signals are visualized by LEDs. The adaptor is best connected to the system under test via a set of small clip-on probes, as shown in the introductory photograph. In a number of cases, the adaptor may be connected in parallel to the relevant lines in the system under test. That can be done by virtue of the high current capacity of the HCT541. In effect, the 541's signals will simply override the clock and RST signals in the system.

The 5-V supply voltage for the test adaptor should be taken from the system under test, and connected permanently before the latter is powered up. Separate supplies must not be used because the order in which the circuits are switched on then becomes an important factor to the microcontroller.

Connecting up to the 80C32 SBC

To illustrate the practical use of the test adaptor, we use the popular '80C32 single-board computer' (SBC) described in Ref. 2 as an example. Interspersed with the descriptions below are hints on how to use the test adaptor with other microcontroller systems.

RESET connection

Many microcontroller systems have a 'reset' push-button, which pulls the processor's reset input, or a control input of a watchdog circuit, high or low. The test adaptor is connected directly to the reset input of the relevant system. The software allows the user to determine the length of the reset pulse, and select between an active-high or active-low reset pulse level.

The 'case' for the 80C32 SBC looks as sketched in **Fig. 2**. The adaptor controls the reset input by charging and discharging a capacitor. The (simple) logic analyser incorporated in the software which runs on the PC has adjustable safety margins as regards the length of the reset pulse. This is done to make sure that the processor is out of its reset state when it is clocked and monitored. During reset, the software generates the clock pulses needed by the 8051/80C32.

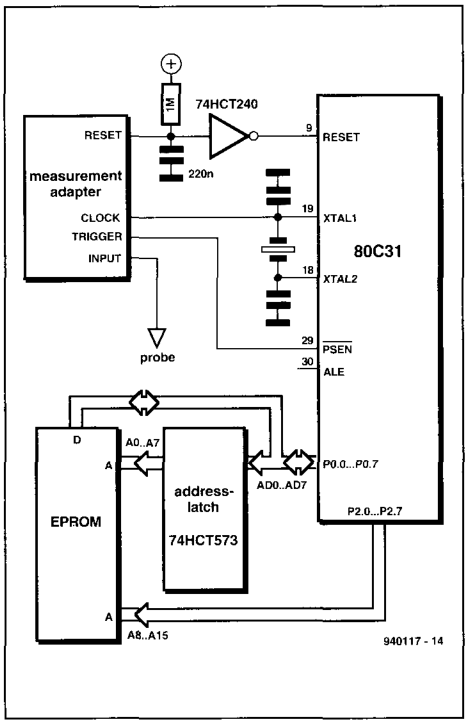


Fig. 2. Connecting the analyser to the test adaptor.

CLOCK signal

The clock signal supplied by the adaptor is used to clock the processor in the system under test, see **Fig. 2** again. In most cases, an externally connected quartz crystal is used to supply the system clock in conjunction with the on-chip oscillator. The CLOCK output of the adaptor is simply connected to one of the quartz connections. With the 40-pin DIL package 8051, pin 19 is recommended. Different pin numbers may be have to be used with other (N or C-MOS) processors. Use the data sheets to make sure of the connection.

TRIGGER input

If an 8051-based system is under test, this input should be connected to the PSEN line of the processor. The logic analyser software uses the trigger signal to start the actual measurement and analysis. The software allows you to select between a high or low trigger level. With the 8051, 'trigger-polarity low' is selected because any program memory access is flagged by PSEN going low. With other controller systems, a connection to the read or write line may be useful.

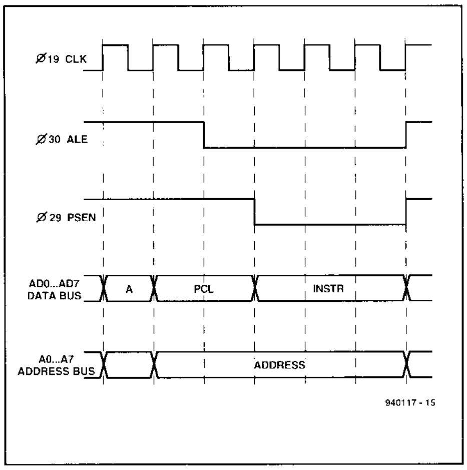


Fig. 3. This is how an 8051 should read from an EPROM.

INPUT connection
INPUT is the test probe proper of the analyser. It is used to connect to various signals in the system, one at a time, for analysis on the PC. For instance, all data bus or address bus lines can be picked one by one. Thanks to the advanced storage and display options of the analyser software, these signals (17, plus CLOCK) may be watched simultaneously on the PC monitor. That enables you to see exactly which data is present on the bus at a specific time. Switch S1 is used to set the non-actuated level of INPUT, for instance, if it is connected to a bus line which can go into high-Z state. In position 'high', the analyser sees a logic high level. In position 'AUTO', it sees the CLOCK signal. In this way, the analyser software is capable of establishing that a line is in high-Z state.

Mini logic analyser software

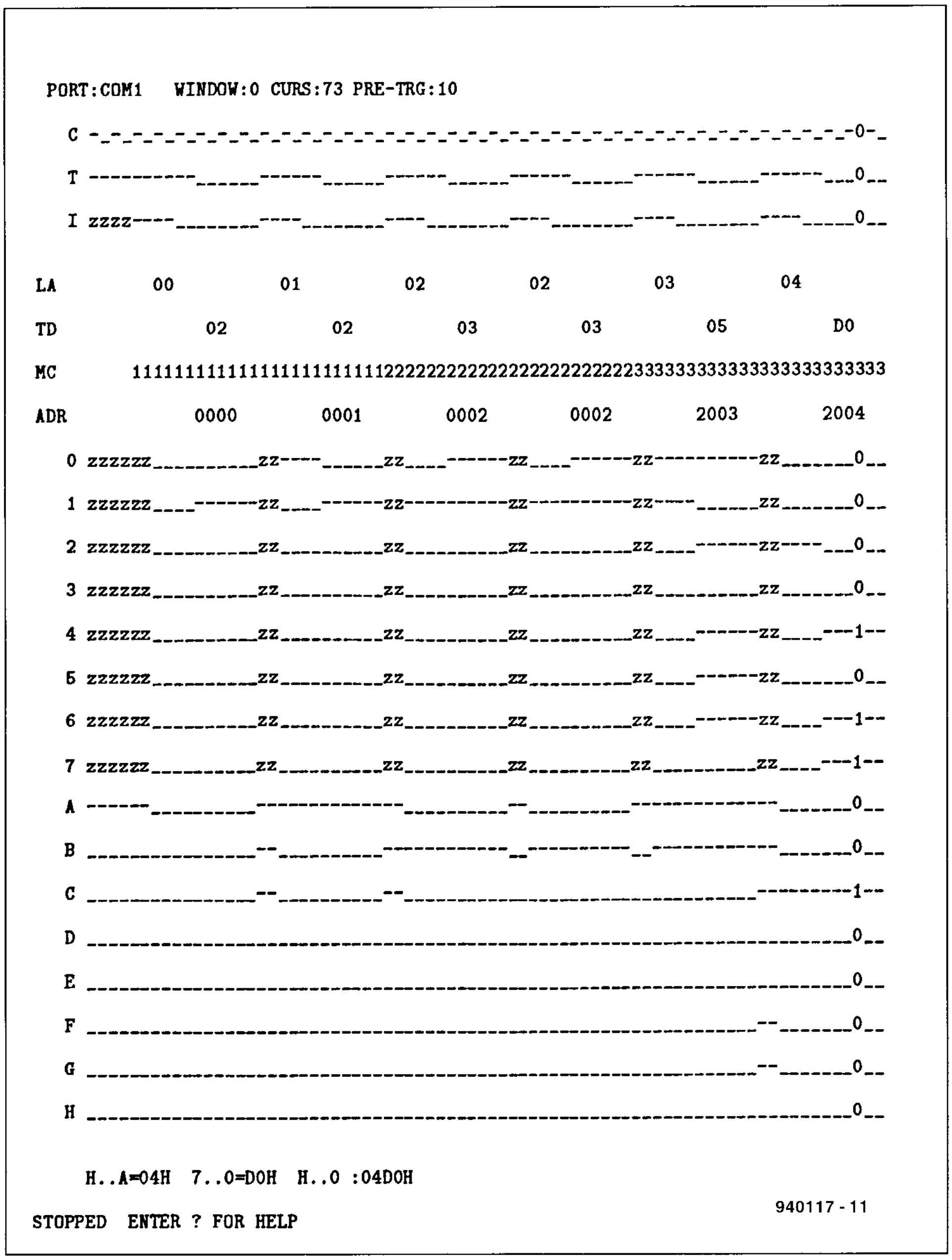
The simpler the hardware, the more powerful the associated software. The test adaptor is linked to the PC via a standard RS232 cable with pin-to-pin connections. The test probes are not connected yet, because the software has to be started first. The analyser software on being run starts by loading a configuration file (if found), which contains the selected operating parameters. Next, the analysis is started. Since the test probes are not connected yet, the software reports a trigger error. Now press some keys to see the main functions of the test system. Type **?** to get a list of the available commands and functions, and also to go into adaptor test mode, which should be run before hooking up the probes to the microcontroller system. On returning to 'normal' mode, you are ready to commence the measurement proper.

The measurement cycle

The measurement cycle starts by actuating the RESET line. In our example, the reset line must be active low. Next, the PC waits a period of which the length (in ms) is set by the RESET-ON parameter. The delay serves to await the charging or discharging of a capacitor which is nearly always present on the reset line in the system under test. Next, the PC generates clock pulses, because most microcontrollers, including the 8051, require a clock signal to complete the reset cycle. The number of clock cycles produced by the PC is defined by the value of the RESET-CYCLES parameter. You can also define whether a clock cycle means 'low-to-high' or 'high-to-low'. Next, the measurement proper starts with the so-called PRE-TRIGGER phase. Clock cycles are then generated by the PC. After changing the level on the CLOCK line, the PC waits a short while before measuring the levels of the TRIGGER and INPUT lines. The relevant values are written into the PC's memory. The RESET line is held low (actuated) for a period whose length corresponds to the value assigned to the RESET-CYCLES parameter. The pre-trigger phase ends when the TRIGGER level drops low. From then on, the processor is running.

The signals measured from then on are captured, stored in the PC's memory, and displayed later. If the trigger signal fails to toggle after a certain time, (TRIGGER-TIMEOUT), the PC ends the pre-trigger phase of its own.

After triggering, the RUN phase



```
 PORT:COM1   WINDOW:0 CURS:73 PRE-TRG:10

   C -_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-0-_

   T ----------______------______------______------______------______------__0__

   I zzzz----________----________----________----________----________----____0__

LA         00          01          02          02          03          04

TD              02          02          03          03          05          D0

MC       111111111111111111111112222222222222222222222223333333333333333333333333

ADR            0000        0001        0002        0002        2003        2004

   0 zzzzzz__________zz----______zz____------zz____------zz----------zz______0__

   1 zzzzzz____------zz____------zz----------zz----------zz----______zz______0__

   2 zzzzzz__________zz__________zz__________zz__________zz____------zz----__0__

   3 zzzzzz__________zz__________zz__________zz__________zz__________zz______0__

   4 zzzzzz__________zz__________zz__________zz__________zz____------zz___---1--

   5 zzzzzz__________zz__________zz__________zz__________zz____------zz______0__

   6 zzzzzz__________zz__________zz__________zz__________zz____------zz___---1--

   7 zzzzzz__________zz__________zz__________zz__________zz__________zz___---1--

   A ------__________--------------__________--__________--------------______0__

   B ________________--__________------------__----------__------------______0__

   C ________________--__________--_________________________________---------1--

   D ________________________________________________________________________0__

   E ________________________________________________________________________0__

   F _______________________________________________________________--_______0__

   G _______________________________________________________________--_______0__

   H ________________________________________________________________________0__


    H..A=04H  7..0=D0H  H..0 :04D0H

STOPPED  ENTER ? FOR HELP
```

940117 - 11

Fig. 4. Screendump produced by the Analysator software. The object is a 80C31 processor starting the EMON51 monitor.

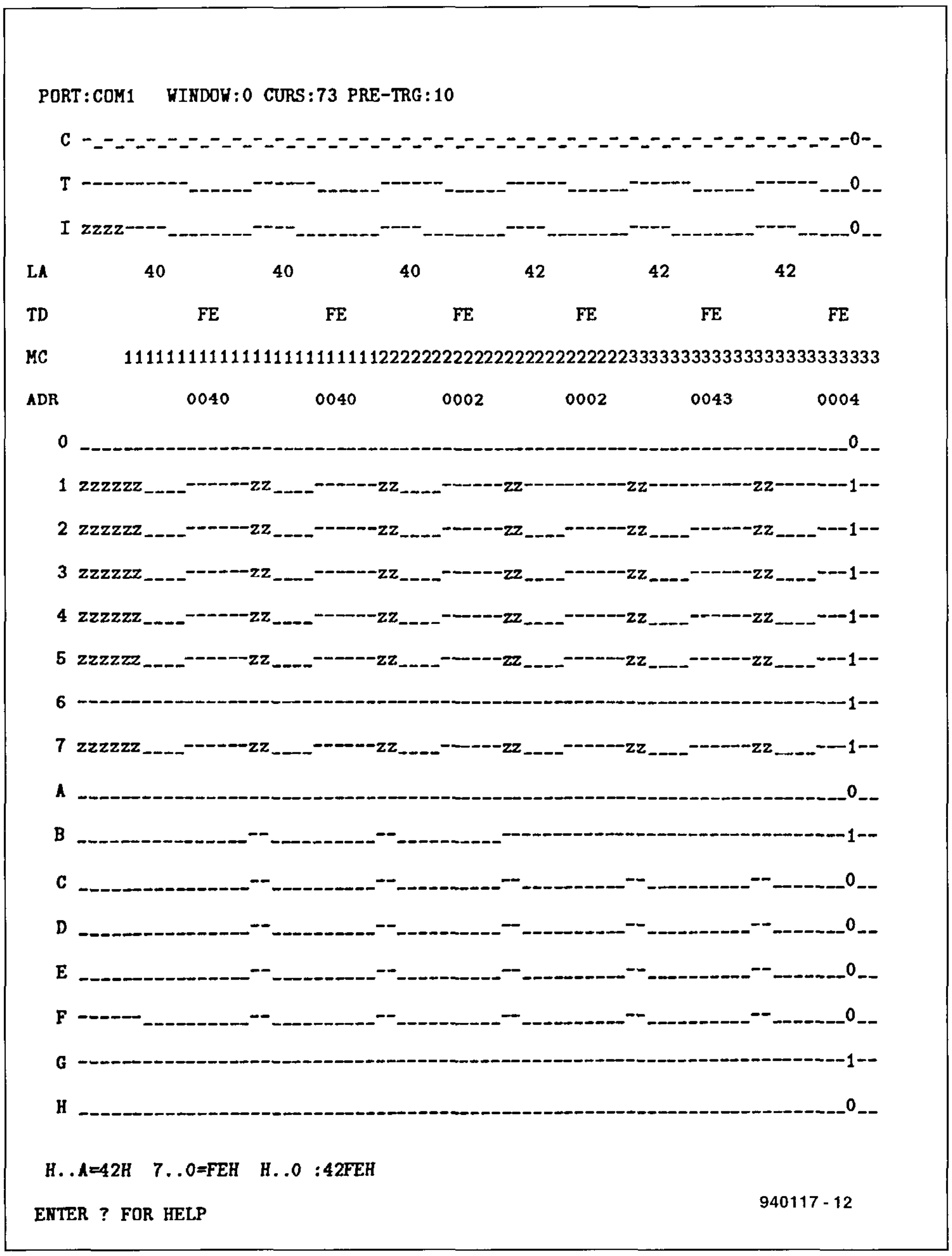
starts. The PC continues to supply clock pulses. The number of these pulses is defined by the STORAGE DEPTH parameter — the maximum value is 3,000. The levels measured by the TRIGGER and INPUT probes are captured and stored into the PC's memory.

Next, the display phase is started. The chronograms for CLOCK, TRIGGER and INPUT are displayed on the top three lines of the screen. The lines below show memorized signals labelled 0 through 7, and A through H. To copy the current INPUT signal to, say, memory '6', simply press the corresponding number on the PC. To be able to view all eight datalines at the same time, start by sampling databus line DB0, until a stable signal is obtained on the PC screen. Next, copy the signal to memory '0'. Do the same for the other databus lines, copying their timing diagrams to the respective memories.

A cursor function is available to get a better view of the state of a number of signals at a specific time. The current level of the lines is marked by a '1' or a '0' at the cursor location. The upper line on the PC screen shows the state of the eight signals 0 through 7 or A through H in hexadecimal notation, allowing single addresses and data to be traced in a comfortable way. The entire screen can be scrolled horizontally to enable the results of longer test periods to be examined also.

High-Z recognition

Bus lines in microcontroller systems can be switched high, low or to a high-impedance (high-Z) state. To be able to detect the latter state reliably, a slightly better measurement method is actually required than offered by the present test adaptor. Fortunately, there is a trick to overcome the adaptor's limitation in this respect. Assuming that there are no propagation delays, a logic signal in a microcontroller system can only change on a clock transition, while it remains steady during a clock cycle. With S1 set to AUTO-Z, and INPUT connected to a bus line in high-Z mode, the level at INPUT changes in the middle of the clock cycle. Provided AUTO-Z is selected, the analyser software is capable of detecting this, and putting a **z** at the appropriate location on the PC screen. In this way, open-circuited IC inputs are also detected. It should be noted, however, that the high-Z detector functions only if the 'cycle' has been defined properly (low-high or high-low). Because of their relatively high-value pull-up resistors, port lines of the 8051 which produce a 1 (high level) are also marked as 'high-Z'.



```
PORT:COM1   WINDOW:0 CURS:73 PRE-TRG:10

   C -_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-_-0-_

   T ----------______------______------______------______------______------___0__

   I zzzz----________----________----________----________----________----_____0__

LA          40          40          40          42          42          42

TD               FE          FE          FE          FE          FE          FE

MC        1111111111111111111111122222222222222222222222223333333333333333333333333

ADR              0040        0040        0002        0002        0043        0004

   0 __________________________________________________________________________0__

   1 zzzzzz____------zz____------zz____------zz----------zz----------zz--------1--

   2 zzzzzz____------zz____------zz____------zz____------zz____------zz____---1--

   3 zzzzzz____------zz____------zz____------zz____------zz____------zz____---1--

   4 zzzzzz____------zz____------zz____------zz____------zz____------zz____---1--

   5 zzzzzz____------zz____------zz____------zz____------zz____------zz____---1--

   6 --------------------------------------------------------------------------1--

   7 zzzzzz____------zz____------zz____------zz____------zz____------zz____---1--

   A __________________________________________________________________________0__

   B _______________--__________--__________-----------------------------------1--

   C _______________--__________--__________--__________--__________--_______0__

   D _______________--__________--__________--__________--__________--_______0__

   E _______________--__________--__________--__________--__________--_______0__

   F ------__________--__________--__________--__________--__________--_______0__

   G --------------------------------------------------------------------------1--

   H __________________________________________________________________________0__

 H..A=42H  7..0=FEH  H..0 :42FEH

ENTER ? FOR HELP
```

Fig. 5. The same as Fig. 4, but this time with two (purposely made) hardware errors on the board.

Example analysis

An example analysis will be carried out on a properly working 80C32 SBC fitted with an AMD 80C31 controller and an EMON51 system monitor. The first instructions executed by the processor are

```
0000      020203LJMP 203H
0203      75D000MOV PSW,#0
```

The timing diagram in **Fig. 3** shows how an 8051 gets access to the contents of an EPROM. Provided no read or write operation is performed in the external data memory, two program memory access operations occur in every machine cycle. Each machine cycle has a length of 12 clock oscillator clock cycles. An MCS-51 instruction takes either one or two machine cycles (except the MUL and DIV instructions). So, a memory access operation takes six oscillator periods. During the first period, the databus is in high-Z mode, while ALE and PSEN are logic high. During the next two periods, the lower-order address byte is switched to the multiplexed data/address bus. When ALE has dropped low, the value is stored in the address latch during periods 3 through 6. During periods 4, 5 and 6, PSEN drops low also, which marks that the EPROM has actually copied its data on to the databus.

Let us continue to trace the individual instructions with the aid of the screendump shown in **Fig. 4**. To assist in understanding what the multitude of data is all about, the lines LA (lower address), TD (transferred data), MC (machine cycle) and ADR (address)

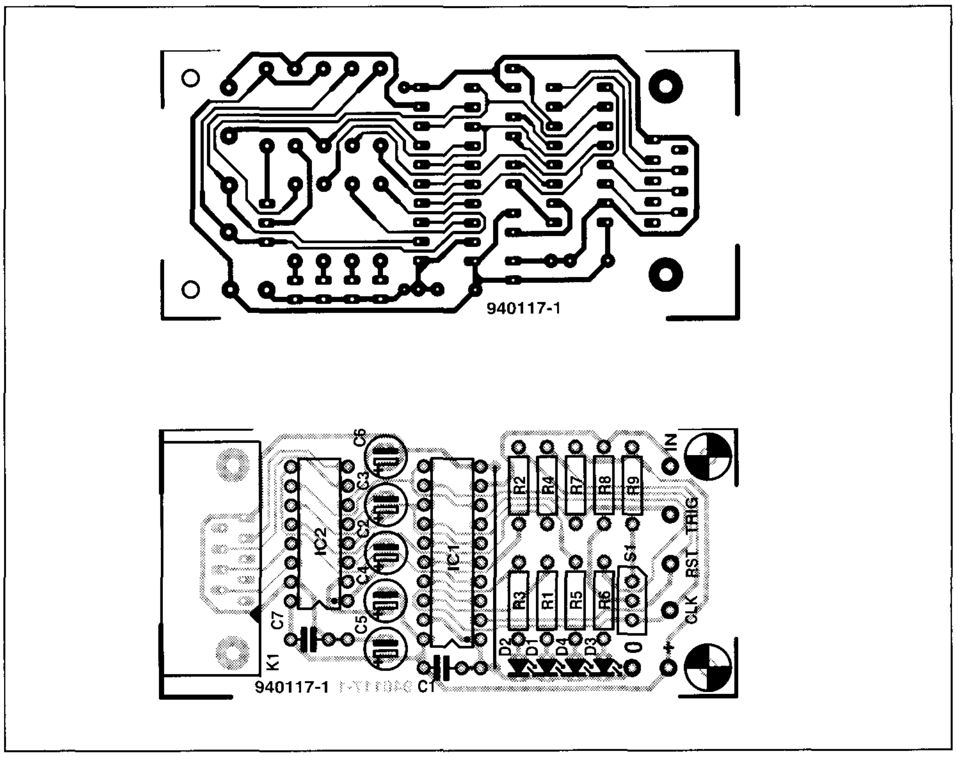


Fig. 6. Track layout and component mounting plan of the printed circuit board designed for the test adaptor (board available ready-made through the Readers Services).

COMPONENTS LIST

Resistors:
R1;R3;R5;R6 = 470Ω
R2;R4 = 1kΩ

Capacitors:
C1;C7 = 100nF
C2-C6 = 10µF 16V radial

Semiconductors:
D1-D4 = LED, 3mm
IC1 = 74HCT541
IC2 = MAX232

Miscellaneous:
K1 = 9-way Sub-D socket, PCB mount
S1 = miniature switch, SPDT, PCB mount, or 3-way jumper
PCB and software on disk: order code 940117-C (see page 70).
Software on disk also available separately, order code 946203-1 (see page 78).

were added manually. The first line, C, shows the clock signal of the 80C31. Then comes the PSEN signal on the T (trigger) line. The INPUT line, I, shows the ALE signal. Memory lines 0 through 7 contain the levels captured on the multiplexed address/data bus. Signals A through H show the eight low-order address lines of the EPROM. The first access to the EPROM for the first instruction starts on the third clock period. This instruction, LJMP (opcode: 02), is read from address 0000 in the EPROM. During the next EPROM access operation, the 80C31 fetches the first (high-order) byte of the jump address from address 0001 in the EPROM. Next, the second machine cycle of the LJMP instruction starts. During the first EPROM access operation of this cycle, the low-order byte of the jump address (value: 03H) is fetched from EPROM address 0002. The second access is a dummy operation, again fetching the code 03H from address 0002. These dummy operations are typical of the 8051 family of microcontrollers, and tend to complicate the reading operations for the desired signals.

During the next machine cycle, the instruction MOV PSW,#0 is executed. The next two EPROM access operations transfer the bytes 75H and D0H correctly. The complete address can not be determined on the basis of the displayed signals, because the high-order address byte is not captured. If desired, that may be done in a second pass, which is not difficult. Before that is done, however, it is recommended to run a thorough check on all address lines during the first EPROM access operation. As you can see, the system allows each step of the microcontroller to be traced with great accuracy.

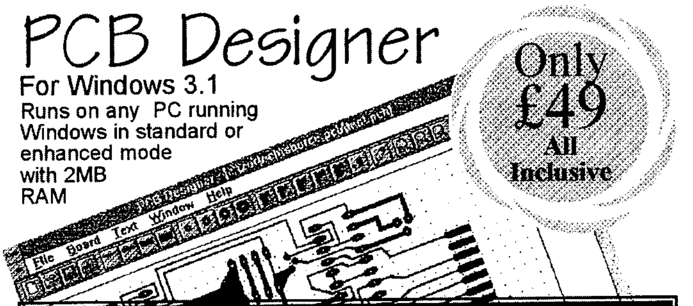
Finding the error

Let us deliberately create a fault on the 80C32 SBC, and see what happens if we hook up this board to the present test system. Looking at multiplexed address/data bus as part of the analysis shown in **Fig. 5**, it is seen that AD0 remains low all the time, and AD6, high. Apparently, these lines never go into high-Z state. And that, you guessed it, pinpoints the errors on the board: address line AD0 is short-circuited to ground, and AD6 to +5 V. Incidentally, the high-order addresses (port P2 of the 80C31) must always be at 00H.

Now let us see what the processor is actually doing during the first few cycles. The first ALE-low condition causes a value 40H to be written into address latch. Although the 80C31 has produced the value 00, the permanently high level of AD6 causes a wrong address to be copied to the address latch. Although the EMON51 EPROM contains the value 'FFH' at address 40H, the processor actually reads back 'FEH' because AD0 is permanently low. The opcode 0FEH happens to mean: MOV R6,A, is one machine cycle long, and occupies one byte. Consequently, the second EPROM access operation in the first machine cycle is nothing but a dummy. Next comes the second machine cycle, which yields the second instruction. At this stage the instruction counter in the 80C31 reads '1'. However, since AD0 is at 0 all the time, the address latch is again loaded with the value '40H'. Subsequently, another opcode '0FEH' is fetched. The dummy memory access operation with this instruction, by the way, is to address 42H this time, as a result of the changed state of the instruction counter. This address in the EPROM again contains 'FFH', which is read as 'FEH' by the processor. Another 'MOV R6,A' instruction is executed without making any sense. This continues endlessly until the hardware fault is removed and the system is reset.

As shown above, apparently simple hardware errors may cause rare and very hard to understand signals. That is why there is a golden rule in microcontroller debugging: if you find a hardware error, eliminate it. Do not try to understand what it does to the software; pursuing that cause is often trivial and a waste of time.

Finally, those of you who are struggling with a faulty 80C32 single-board computer running the EMON51 monitor may use the screendump in **Fig. 4** as a reference to see how the system **should** start up after a reset.



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Other applications

Debugging an 8051-based microcontroller system often involves testing RAM and port access operations also. Here, it pays to use an EPROM emulator into which a short test program is blown. To test port P1, for instance, the following little program is used:

```
start       INC     P1
            SJMP    start
```

Similarly, check write operations to, say, address 2345H with the aid of the following program:

```
start       MOV     DPTR,#2345H
            MOV     A,#0A5H
            MOVX    @DPTR,A
            SJMP    start
```

In some cases, it is desirable to view more cycles at the same time. Fortunately, that is catered for by the program.

The operation of the **80C535 single-board computer** (Ref. 3) can be analysed without problems using the present system if you set the 'cycle' definition parameter to LOW-HIGH, and inject CLOCK at pin 39 of the CPU.

The use of the 'Analystor' program and the associated measurement adaptor is not limited to microcontroller boards. In fact, the tester may be used with almost any logic circuit which can be made to work from an externally applied clock. In the worst case, a PCB track or two may have to cut to enable the clock signal to be injected. Circuits that can be analysed and debugged in this way. include those containing counters, PALs or GALs.

It will be clear that the present debugging system is simple, and will not enable you to find any error 'spot-on'. With a little dexterity, however, most, if not all, malfunctions can be recognized. A broken PCB track, for instance, may cause one and the same signal to look different at two different points in the circuit. So, check if two (supposedly) equal signals are actually equal. Short-circuits between data bus lines may also be quite elusive and pose baffling problems.

Construction

The test adaptor is best built on the printed-circuit board shown in **Fig. 6**. This board and the associated Analysator software is available ready-made through our Readers Services. The board is fitted in a small plastic box. The 'external' elements are the 9-way sub-D socket, switch S_1, wires for the 5-V supply from the system under test, the four probe wires and the associated LEDs. (940117)

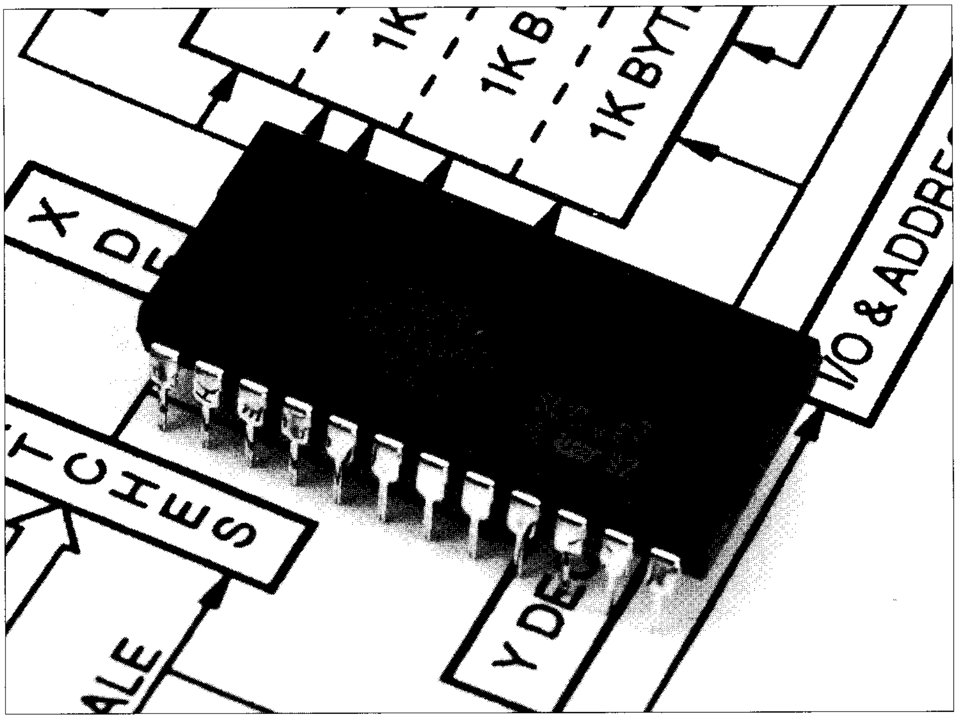
References:

1. 80C32.8051AH-BASIC Single-board computer, *Elektor Electronics* May 1991.
2. Short course 8051/8032 microcontrollers and assembler, Elektor Electronics (Publishing) book, ISBN 0 905705 38 6.
3. 80C535 Single-board computer, *Elektor Electronics* February 1994.

More on the same subject:
Debugging the 8031 series, *Elektor Electronics* November 1994.

SELF-LOADING EEPROM TYPE X88C64

Xicor's X88C64 SLIC™ (self-loading integrated code) IC is an 8Kx8 EEPROM with an internal address decoder and a multiplexed data/address bus. The memory consists of two independent arrays with a size of 4Kx8. Another special feature of the SLIC™ is that it has a non-volatile code downloader which makes program development a lot easier for the popular 80xx and 68xx microprocessors.



By our editorial and design staff. Source: Xicor Inc.

COMPLEX and expensive development tools never seem to have boosted the popularity of any microcontroller. In general, the easier-going the software development and debugging tools, the wider the acceptance of a particular device. Arguably, an EPROM emulator is the cheapest development tool which can be used almost universally. One side of the emulator is connected directly to the socket for the EPROM which contains the system software. The other side is connected to a PC which is used to (cross-) assemble, debug, and download machine code to the emulator, using, for instance, the Jedec, IntelHex or Motorola file formats.

Although an EPROM emulator is a cost-effective and fairly easy to handle software development tool, there are easier solutions. Xicor, with the introduction of its X88C64 SLIC EEPROM, shows the way.

Essentially, a microprocessor system in which SLIC routines are used can be programmed via the regular serial interface. The SLIC contains a compact library of routines which are, in principle, started automatically after a reset. The only requirement as regards the machine code is that a 3-byte code block ('header') is transmitted before the data. Software is available for MS-DOS PCs to make IntelHex files compatible with the SLIC protocol.

Both 4-K memory arrays inside the X88C64 contain SLIC routines. Version Beta 2.1 has 256 instructions in the upper part of the memory bank (1F00H - 1FFFH), and 240 bytes in the lower bank's address range, just above the interrupt vectors (0030H - 011FH). The address division is shown in **Fig. 1**. The user's application code should avoid these areas as part of its code segment, otherwise it will overwrite the SLIC. All user programs may use the memory segment between 0120H and 1F00H.

The SLIC programming routines form part of the software, and may be found in both memory arrays. During programming, the EEPROM array which is not in use is not accessible for about 5 ms. Consequently, software from the other array has to be used during that period. The X88C64 comes with the reset vector at address 0000H pointing at 0030H, so that the processor jumps to the start of the SLIC segment after a reset. To enable your own program to be launched at power-on, this reset vector has to be overwritten.

To be able to use the SLIC routines again after overwriting the reset vector, the user program has to provide for a jump to these routines. Alternatively, some code may be added to the user program to enable the SLIC routines to be started via, for instance, INT0 or INT1. If you forget to include such a routine, the SLIC is gone forever (well, almost) after programming, so take care! Do not download 'any' program to make your first acquaintance with the X88C64. Familiarize yourself with this new device in a step-by-step manner, making sure at all times that the SLIC routines are not overwritten.

Re-entering the SLIC segments into the EEPROM banks of the X88C64 requires a dedicated programmer which is capable of supplying special codes, and using the multiplexed data/address bus. Copies of the SLIC routines are supplied on disk with the EEPROM.

Conditions

The data sent to the SLIC software must meet a number of conditions. To begin with, a 3-byte header must be transmitted. The headers should consist of:

- command type identifier;
- total number of bytes in data block;
- starting memory address (LSB first).

The subsequent data must lie in the same memory block (page) of 32 bytes. The databytes are read by the software, and stored into the internal RAM. Next, all interrupts, including those of the UART, are blocked. Then, the data is copied to the EEPROM. Programming the entire block takes just as long as programming a single byte. During programming, all data transmitted to the UART are lost. Hence, new data may not be transmitted until the SLIC software reports that it has finished programming. This is indicated by returning a 'D' (for 'done').

The protocol is fairly complex because the EEPROM can not be read if data is being written into the same block. If data is being written into the lower block (0000H), the processor must fetch its instructions from the other block (upper part of the memory). Since the vectors, like the instructions, are stored in EEPROM, it is not possible to read them during programming (notably the UART vectors). That also explains why the serial link is 'temporarily out of order' during programming.

The SLIC software remains intact after you have changed the interrupt vector. The first thing it does on being actuated is reprogram the UART interrupt vector. This re-programming operation is performed after each reset, power-up, or call to the SLIC program. There is one limitation, though: according to Xicor, the maximum number of erase/write operations on an EEPROM memory location is 10,000.

The complete system

The SLIC program written by Xicor has a size of about 500 bytes, and consists of two parts. The part in the lower half of the EEPROM is capable of programming the upper half, and vice versa. EEPROMs with the code 'SLIC' printed on them have these programs. Empty EEPROMs are also available from Xicor.

You are ready to start programming as soon as the EEPROM is fitted into the system. Set your PC or terminal for 9600 baud, 8 databits, no parity and 1 stopbit. Commands are issued by transmitting an ASCII character to the SLIC. These characters may be terminated with a carriage return (CR), although that is not strictly necessary. The SLIC responds as described below. Usually, it does not generate a CR; and never a line feed (LF). The SLIC routine is started after a hardware reset. First, a 'D' is returned to the PC. If you do not see this character, there is something wrong in the system.

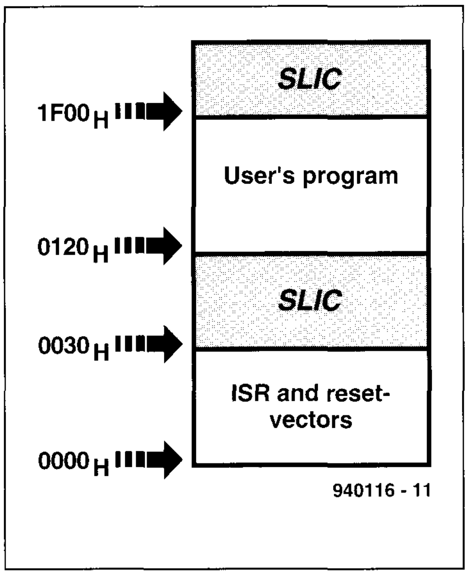


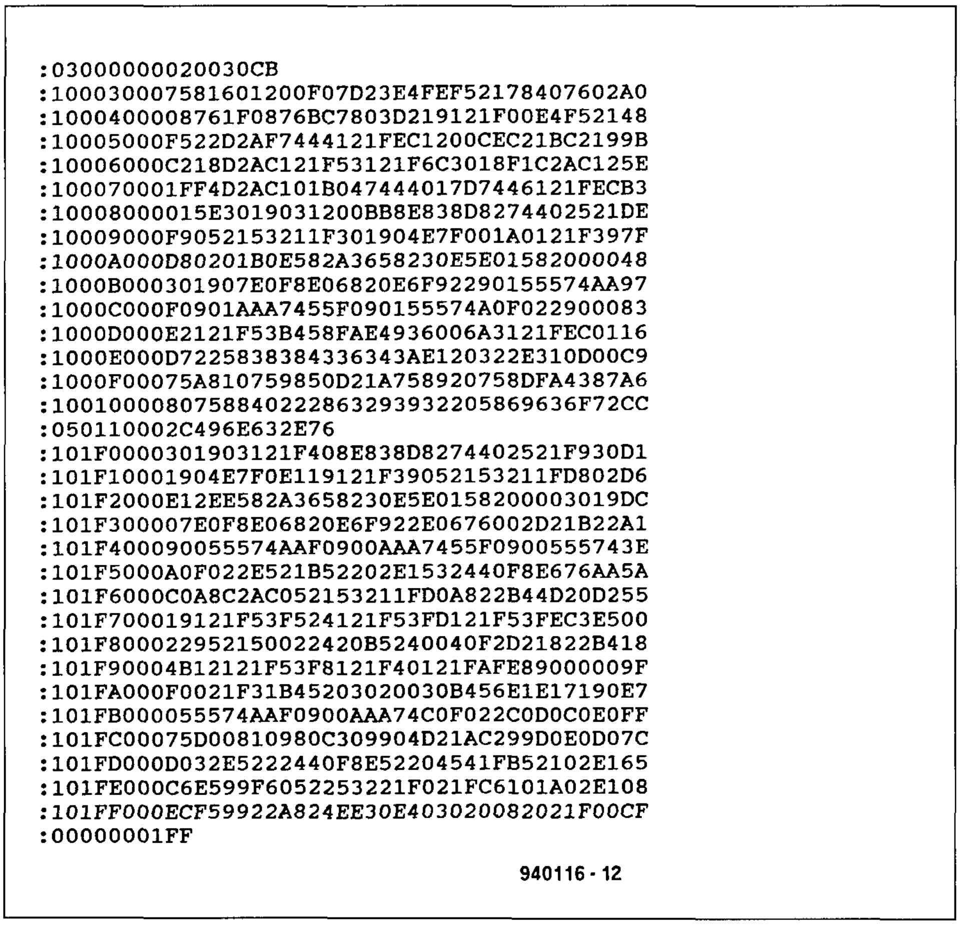
Fig. 1. EEPROM memory division.

After the reset (hardware or software), the following command must always be sent:

Command: **X**
Response: **X88C64:β2.1** (CR)
The SLIC responds to this command by returning its version number (here: Beta 2.1) after a colon. Next, one of the following commands may be sent:

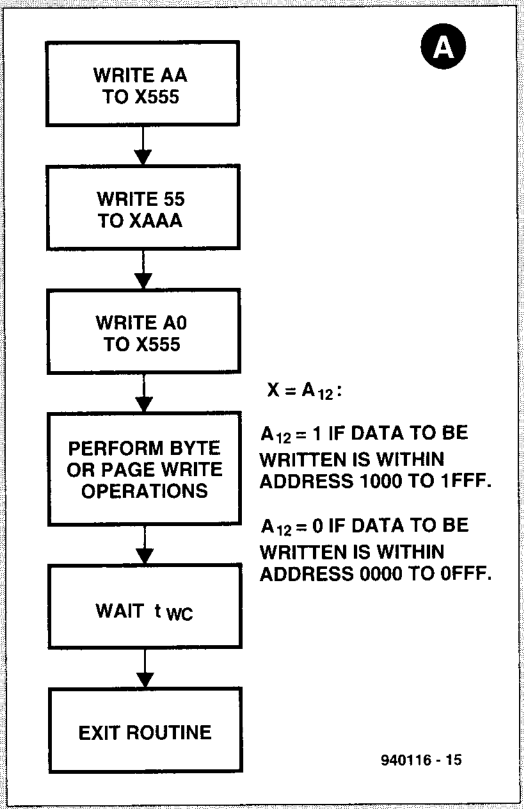
Command: **Mxxxdata**
Response: **D**
Program (Modify) the contents of the EEPROM. The capital M must be followed by a byte (represented by the first 'x') which indicates the number of bytes to be programmed. The second 'x' represents the LSB (least-significant byte) of the programming address. The third 'x' is the MSB (most-significant byte) of the address. Next come the data. Any number between 0 and 255 is transmitted as a byte. There is no error detection or correction.

The following points should be observed when programming. The number of bytes may be between 1 and 32. If you program a single byte, any address may be given. If you program more bytes, the SLIC routine will first receive them and then store them in a buffer. Once all bytes are received, the EEPROM is programmed in 'page' mode. In this time-saving mode, up to 32 bytes are sent to the EEPROM, and programmed in one go within 5 ms. This system works properly if the data-



```
:03000000020030CB
:10003000758160120OF07D23E4FEF52178407602A0
```

Fig. 2. Example of an IntelHex file. This is actually the code contained in the SLIC.


A
WRITE AA TO X555
WRITE 55 TO XAAA
WRITE A0 TO X555
PERFORM BYTE OR PAGE WRITE OPERATIONS
WAIT t WC
EXIT ROUTINE
X = A12:
A12 = 1 IF DATA TO BE WRITTEN IS WITHIN ADDRESS 1000 TO 1FFF.
A12 = 0 IF DATA TO BE WRITTEN IS WITHIN ADDRESS 0000 TO 0FFF.
940116 - 15

X88C64 SLIC EEPROM

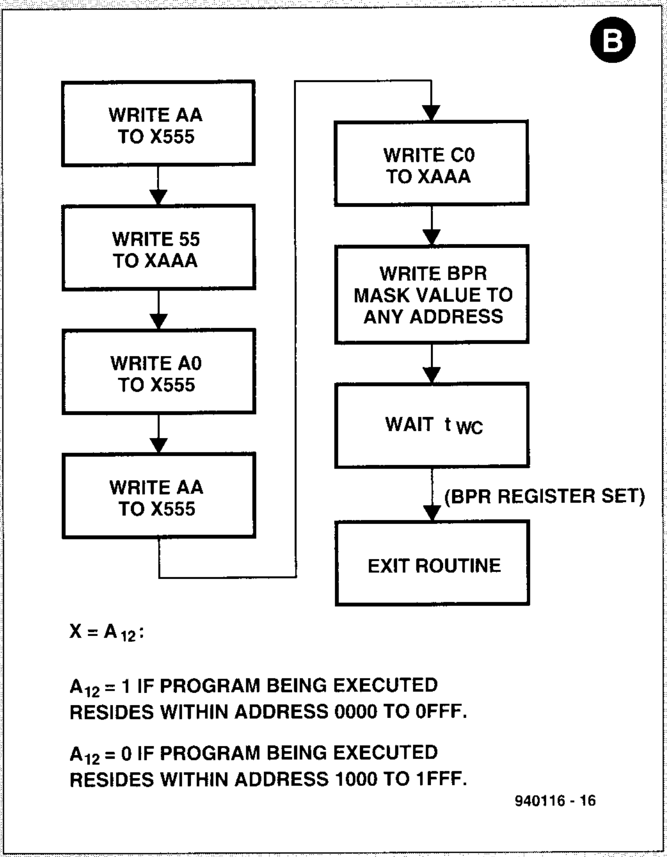
Xicor's X88C64 EEPROM has a couple of features which set it apart from other EEPROMs. The main difference is the multiplexed address/data bus, which enables the device to be connected directly, without a latch, to the processor bus of 8031-series processors. Xicor also supply the X68C64 which is designed to connect to 68xx processors such as the 68HC11. The EEPROM consists of two 4Kx8 memory arrays which can be individually read and programmed. There are two ways to protect the data in the memory:

SDP, protection via software. This serves to prevent bytes being overwritten by accident. Programming is only allowed after three pre-defined bytes have been written to three pre-defined addresses. See the flow diagram in **Fig. A**.

BPR, extra protection of parts of the EEPROM (chunks of 1 KByte each). This is achieved by writing five pre-defined bytes to five pre-defined addresses. See the flow diagram in **Fig. B**.

Internally, the EEPROM consists of two independent arrays which can be read and programmed without affecting one another. To enable the microcontroller program to be modified without removing the EEPROM from its socket, a system configuration as shown in **Fig. C** has been designed. The structure of the processor-EEPROM interface is such that ALE, PSEN, WR and RD are all used. Apart from reading instructions with the aid of the PSEN signal, it is, therefore, also possible to write data to the EEPROM (because of the presence of WR). Reading data is accomplished with the aid of the RD signal.

The EEPROM actually consists of two 4Kx8 EEPROM arrays which will be referred to as 'upper' and 'lower' for the sake of convenience. When he processor is busy reading instructions from the lower array, the upper array is not used, and may be programmed. Programming takes a maximum of 5 ms, during which it is not possible for the microprocessor to fetch instructions from the relevant array. As already mentioned, programming always takes place within the bounds of a page, i.e., 32 bytes. As soon as a byte is written within such a page, the information is stored in a latch inside the EEPROM. The processor may then write the next byte to the same page. The bytes may arrive with intervals of a couple of microseconds. If no new information is written into the memory page within 100 μs, the actual programming operation commences. During this operation, the EEPROM is not accessible for a period of up to 5 ms. In practice, programming will take less than 5 ms. Hence, a protocol is incorporated which checks if the programming is finished. The level on data line 6 toggles during programming. The programming operation is finished if the same level appears twice in succession on the line.


B
WRITE AA TO X555
WRITE 55 TO XAAA
WRITE A0 TO X555
WRITE AA TO X555
WRITE C0 TO XAAA
WRITE BPR MASK VALUE TO ANY ADDRESS
WAIT t WC
(BPR REGISTER SET)
EXIT ROUTINE
X = A12:
A12 = 1 IF PROGRAM BEING EXECUTED RESIDES WITHIN ADDRESS 0000 TO 0FFF.
A12 = 0 IF PROGRAM BEING EXECUTED RESIDES WITHIN ADDRESS 1000 TO 1FFF.
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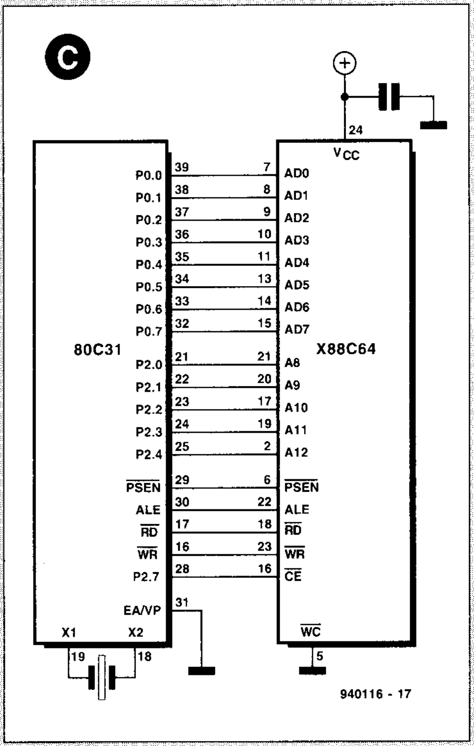

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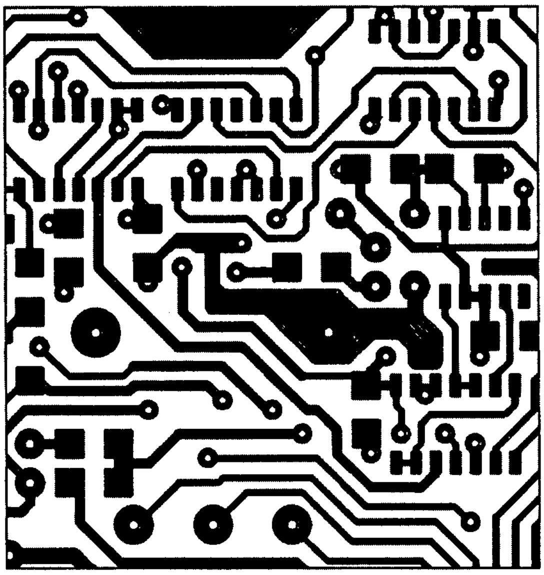

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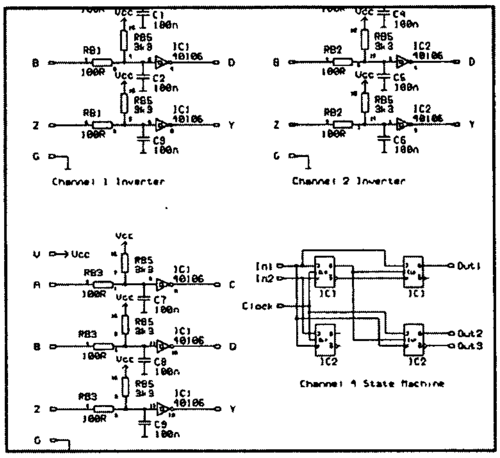

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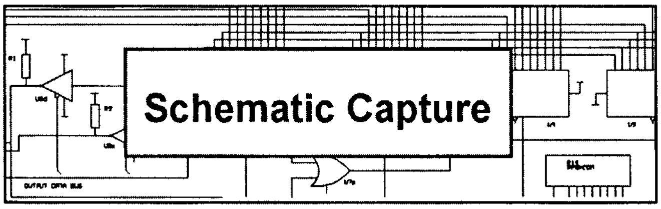
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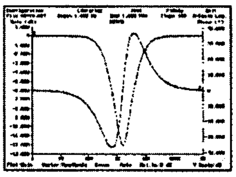
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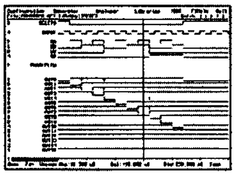

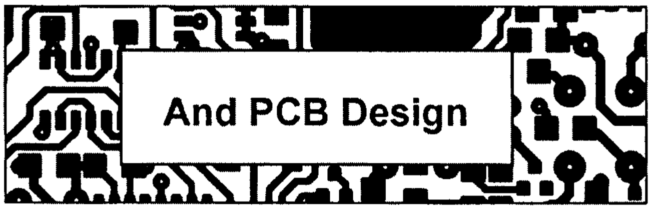
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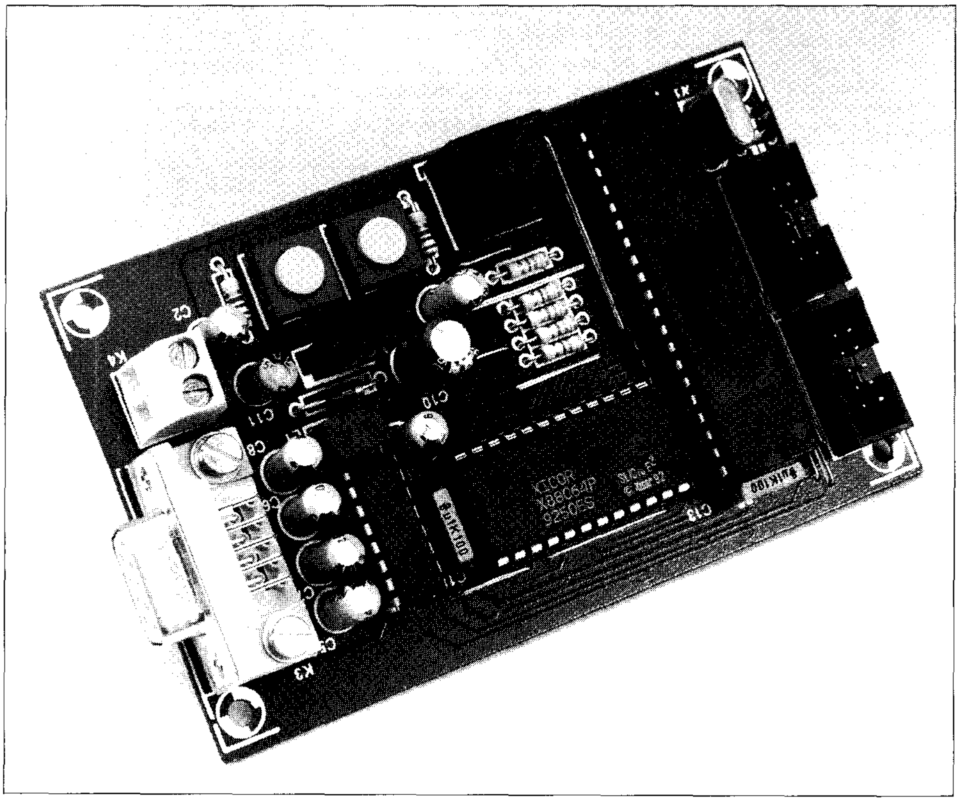
```
REM SIMPLE TEST FOR SLIC
CLOSE #1
CLS
OPEN "COM1:9600,N,8,1" FOR RANDOM AS #1
PRINT "PLEASE PUSH RESET BUTTON"
PRINT INPUT$(1, #1); " RECEIVED"
PRINT "SLIC IS ALIVE, NOW ASKING FOR ID"
PRINT #1, "X"
PRINT "WAITING FOR RESPONSE..."
ID$ = ""
WHILE RES$ <> CHR$(&HD): REM UNTIL <CR>
RES$ = INPUT$(1, #1)
ID$ = ID$ + RES$
PRINT ASC(RES$);
WEND
PRINT : PRINT "THE ID IS "; ID$

PRINT
PRINT "NOW WE DO SOME PROGRAMMING"
REM IF YOU CHANGE NEXT LINE REMEMBER LSB OF ADDRESS FIRST!!
PRINT #1, "M"; CHR$(3); CHR$(&H30); CHR$(5); CHR$(&H12);
CHR$(34); CHR$(56)
PRINT "WAITING FOR RESPONSE"
RES$ = INPUT$(1, #1)
PRINT "RECEIVED IS ";
PRINT RES$; "("; ASC(RES$); ")"

PRINT
PRINT "VERIFICATION OF PROGRAMMED BYTES"
PRINT #1, "V"; CHR$(3); CHR$(48); CHR$(&H5); CHR$(18);
CHR$(&H22); CHR$(56)
PRINT "WAITING FOR RESPONSE"
RES$ = INPUT$(1, #1)
IF RES$ = "F" THEN PRINT "F RECEIVED, VERIFICATION FAILED"
IF RES$ = "D" THEN PRINT "D RECEIVED, VERIFICATION O.K."

CLOSE #1
```

940116 - 13

Fig. 3. A BASIC program which enables the PC to communicate with the SLIC software in an 8031-based microcontroller system.

bytes are intended for addresses which fall into one page. This is the case as long as address lines A5 through A12 remain at the same level. So, take care while programming more than one byte that **only** address lines A0-A4 are allowed to change.



On completion of the programming cycle, the SLIC software returns a 'D' (done). Note that this message only means that the programming operation has been completed. It should not be taken to mean that the data has been programmed correctly.

Command: **Vxxxdata**
Response: **D** or **F**
This command verifies the contents of the EEPROM against the serial databytes. It is largely similar to the 'program' command. Here, too, received bytes are placed into a buffer, and must fall within the same page. The SLIC responds with 'D' (done) or 'F' (fault).

Command: **R**
Response: **D**
Reset command. The X88C64 runs its internal power-up routine and on completion returns a 'D' to the PC. Next, it waits exclusively for 'X'. No response will be given to another reset, a programming or verify command.

Command: **Kdata**
Response: **none**
This command serves to modify the contents of the BPR register. 'Data' indicates the byte written into the BPR register. This determines which blocks are accessible for programming. Each bit determines the 'programming allowed/disallowed' status of a 1-K block (0 = programming allowed; bit 0 is the block with the lowest address).

Fortunately, Xicor supplies a PC program with its SLIC EEPROMs to take the hassle out of the communication protocols described above. The current version (3.34) allows the user to select the COM port used on the PC. Updated versions of the control software may be downloaded from Xicor's bulletin board in the U.S.A. The number is **(+1) 408-9430655.**

The software on being started tells you straight away if communication with the SLIC is possible. If not, go to the setup menu, and select the right communications port. The program requires input data in IntelHex format, which will be available in most cases because it is accepted by most EPROM programmers. The structure is fairly simple: a line starts with a colon. Then follow a number of bytes, the address, a code, the databytes, and, finally, a checksum. **Figure 2** shows a part of such a file.

Since a couple of devices in the 8051 family of microcontrollers have vectors above 0030H, the control program is capable of moving the SLIC segment to address 0080H. Those of you who wish to experiment may find

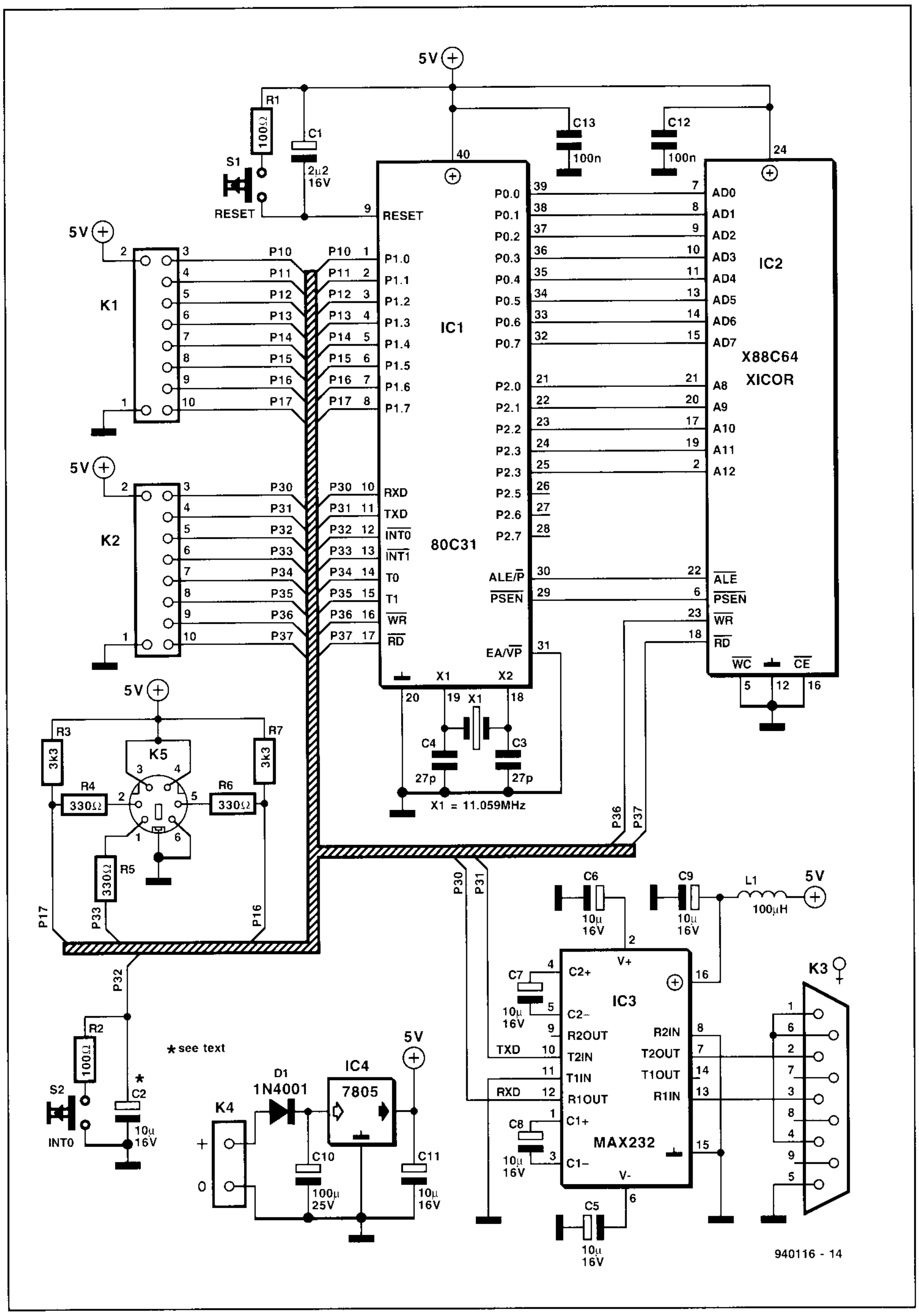


Fig. 4. Circuit diagram of a small 80C31 controller system which incorporates an X88C64 SLIC EEPROM for time-efficient program development.

the BASIC program listed in **Fig. 3** of interest.

The rules of the game

Recapping, observe the following rules when using the SLIC routines:

(1) Supply an IntelHex file.

(2) Do not allow data to cross page boundaries.

(3) Ensure that memory areas 0030H-011FH and 1F00H-1FFFH are not overwritten, because they contain the SLIC.

(4) The UART vector (0023H in the 8031) should be re-programmed in the **last** line of the IntelHex file.

(5) Place a jump to the start of the SLIC code (JMP 0030H) at the INT0 vector address (0003H), and do not forget to enable the INT0 interrupt (bit register EX0=1), and to enable all interrupts (bit register EA=1).

All of this may look pretty complex at first. However, after a while you will become conversant with the programming techniques. Those of you who like (Visual) BASIC or Pascal programming may write a small program which keeps an eye on the above rules, and supplies alerts where necessary. The documentation contained in the SLIC design package also points out that a larger part of the 500 bytes of SLIC program may be incorporated in the user program (for instance, the UART routine). In this way, the SLIC need not be 'ballast' only.

The SLIC design pack supplied by Xicor contains the X88C64, a datasheet, application notes and a diskette containing the above mentioned control program and the source code of the software in the EEPROM.

SLIC demonstration board

Figure 4 shows the circuit diagram of an 80C31 processor board based on an X88C64 SLIC EEPROM. The circuit also contains a MAX232N RS232 driver/interface for the link to the PC, and an I^{2}C interface plus socket. It should be noted that the 80C31 has no built-in I^{2}C software. However, that can be downloaded from the Philips Bulletin Board in Eindhoven, The Netherlands. The number to dial is **(+31) 40 721102**.

The quartz oscillator crystal fre-

COMPONENTS LIST

Resistors:

R$_1$;R$_2$ = 100Ω
R$_3$;R$_7$ = 3kΩ3
R$_4$;R$_5$;R$_6$ = 330Ω

Capacitors:

C$_1$ = 2µF2 16V radial
C$_2$;C$_5$-C$_9$;C$_{11}$ = 10µF 16V radial
C$_3$;C$_4$ = 27pF
C$_{12}$;C$_{13}$ = 100nF

Inductor:

L$_1$ = 100µH

Semiconductors:

D$_1$ = 1N4001
IC$_1$ = 80C31
IC$_2$ = X88C64SLIC (Xicor)
IC$_3$ = MAX232N
IC$_4$ = 7805

Miscellaneous:

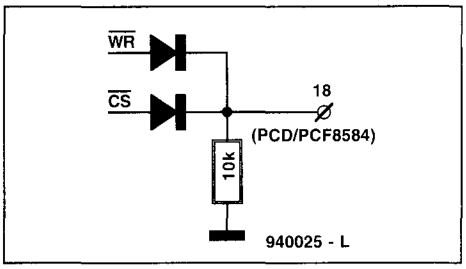
K$_1$;K$_2$ = 10-way boxheader.
K$_3$ = 9-way sub-D socket, angled pins, PCB mount.
K$_4$ = 2-way PCB terminal block, raster 5mm.
K$_5$ = 6-way mini-DIN socket, PCB mount.
S$_1$;S$_2$ = MultiMEC 2CTL2 press-key.
X$_1$ = 11.0592 MHz crystal.
Printed circuit board 940116 (see page 78).

CORRECTIONS AND UPDATES

80C535 Extension card

June 1994, p. 8-11

The PCD8584 may be switched to '6800' mode if a WR signal arrives without a CS signal. The problem may be solved by combining WR and CS in a diode-AND gate as shown below. Pin 18 if IC$_4$ is taken out of the IC socket and connected to ground via a 10-kΩ resistor. The WR signal is found on socket pin 18, and CS on pin 10 of IC$_5$. Also note that the PCD8584 is currently supplied as the PC**F**8584.



Dual-purpose LED display

December 1994, p. 90

Resistor R$_{33}$ should be connected to ground, not to +12 V as shown in the circuit diagram.

Experimentation board for PICs

July/August 1994, p. 74.

In the circuit diagram, the signals on pins 7 and 8 of both connectors K$_1$ should be swapped. MCLR is on pin 8, and RTCC on pin 7. The relevant PCB is all right.

Mains signalling system (2)

May 1994, p. 10-14.

The instructions for command 'T' should read: 'T' must be followed by the address in ASCII, and terminated with a semicolon (';').

The baudrate for the communication software should be set to 300, format: 8 bits, 1 startbit, 1 stop bit, no parity.

Electronic fuse

March 1994, p. 56.

To prevent transistor T$_2$ from burning out when the reset switch is pressed during an overload condition, switch S$_1$ should be connected between the collector of T$_1$ and the base of T$_2$.

quency, 11.0592 MHz, must not be changed into, say, 12 MHz because it determines the speed of the SLIC serial communication (9600 baud). Apart from the reset switch, S$_1$, the circuit also has a press-key to generate an INTO interrupt. If capacitor C$_2$ is made much larger than C$_1$, the circuit generates an INTO interrupt automatically at power-on. This interrupt should cause the system to jump to the SLIC software, via the user program.

The I/O lines of ports 1 and 3 are available on connectors K$_1$ and K$_2$. These connectors may be used to hook up extension circuits which serve to control the 80C31.

Finally, the track layout and component mounting plan of the 80C31/SLIC board are shown in **Fig. 5**. (940116)

For further information, contact
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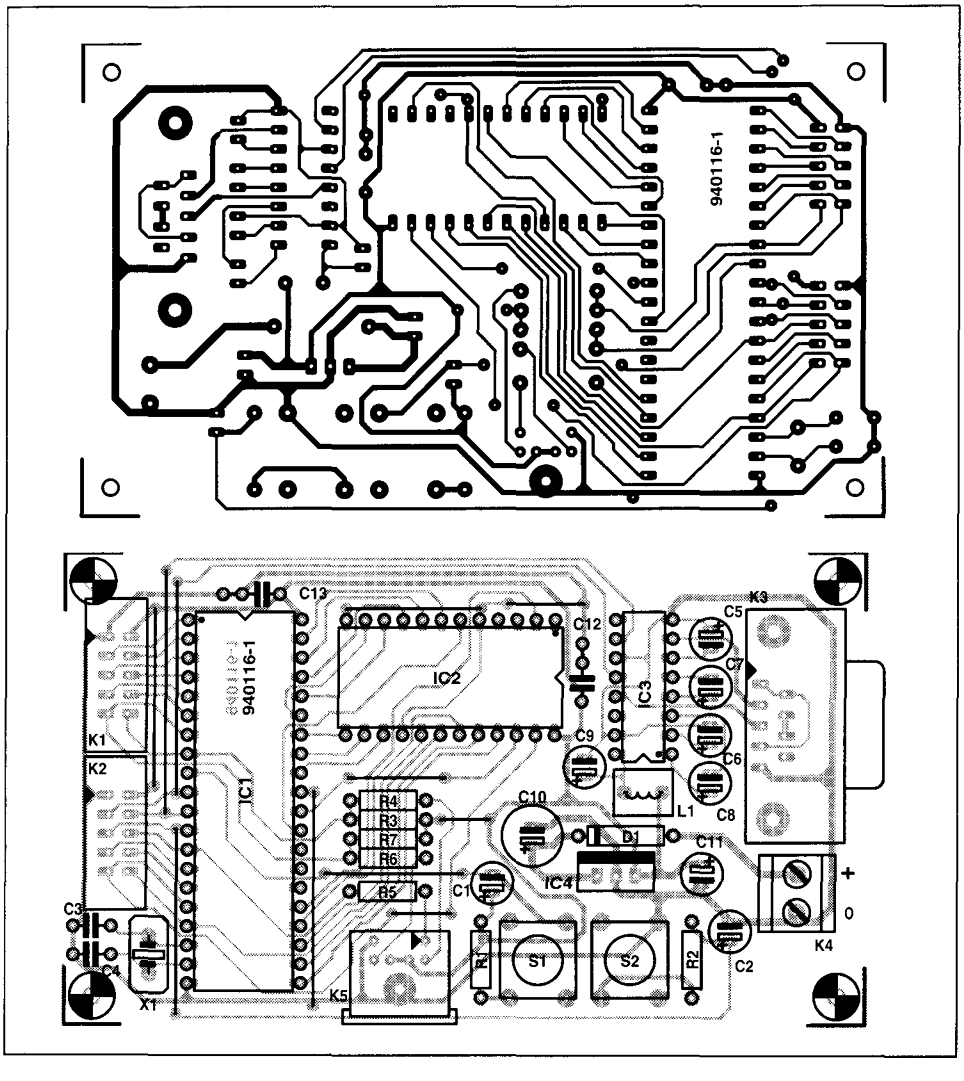

Fig. 5. Printed circuit board designed for the 80C31/SLIC controller (board available ready-made, see page 78).

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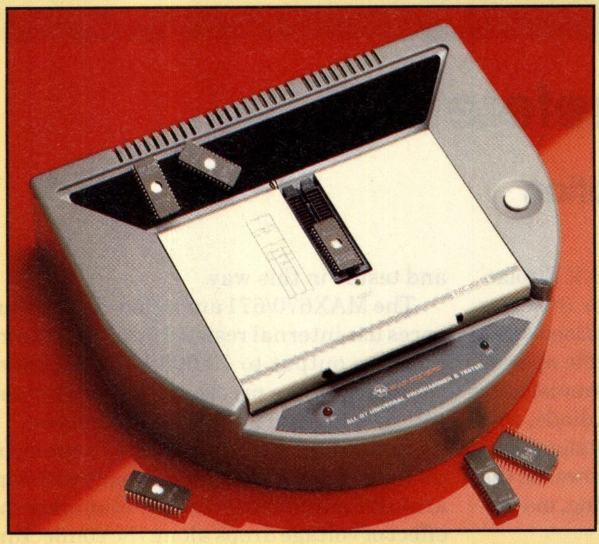

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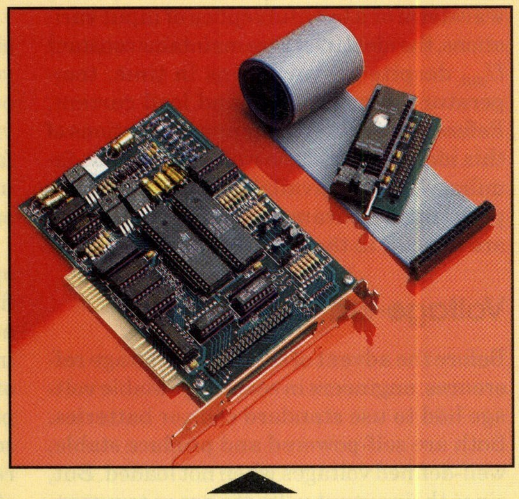

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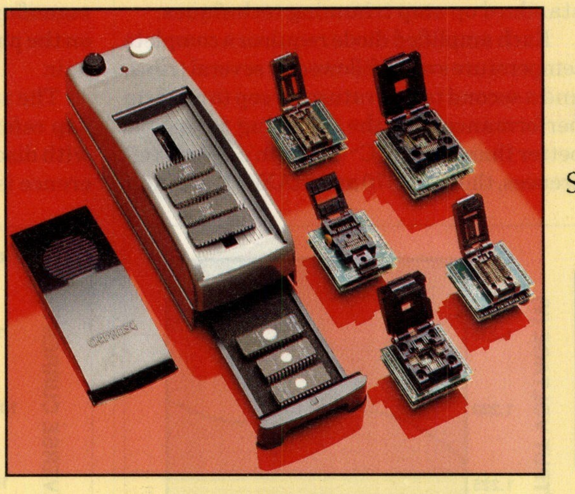

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APPLICATION NOTE

The content of this note is based on information received from manufacturers in the electrical and electronics industries or their representatives and does not imply practical experience by *Elektor Electronics* or its consultants.

Selecting voltage references

A Maxim Application

Voltage references are simple devices, but making the right choice for a given application can be a chore if you do not take an orderly approach. This article simplifies the task with a review of the available reference types and a discussion of the specifications manufacurers use to describe them.

Unlike most electronic circuits, the voltage reference resists any change in output. While most circuits try to produce an ideal waveform or a faithful replica of input variations, the ideal reference maintains constant U_{out} despite all variations in time, temperature, input voltage and load current. References differ in their approximations of this ideal, so to choose well you must be familiar with the available types and their performance parameters. These two topics are covered in the following sections.

Voltage-stable devices

Before the advent of solid-state voltage references, engineers in search of a stable voltage had to use standard cells or batteries. Both are self-powered and produce stable, well-defined voltages when not loaded. But, since their output voltages are so temperature sensitive, they must be specified at a single temperature.

The standard cell consists of liquid mercury and liquid electrolyte in an H-shaped glass container. Though accurate to a few parts per million, it can take weeks or months to recover if overloaded or tipped on its side!

Mercury cells (batteries) are more robust. Good for several years without replacement, they provide about $2\frac{1}{2}$ digit accuracy when new. They furnish only a few milliamps of current. Though still used in some portable applications, most have been replaced by modern low-current (10 fA) references.

The first modern voltage reference is the zener diode. Used mostly in clamp circuits and power supplies, it comes in a variety of voltages, packages, and power ratings. Not quite accurate enough or stable enough to qualify as a voltage reference by itself, the zener produces a reasonably constant voltage when connected in series with a resistor and a source of unregulated voltage.

The zener's temperature coefficient (tempco) is a function of its breakdown voltage, and is remarkably low at about 6.3 V. By placing a conventional pin junction in series with the zener, you get a combination whose forward voltage drop (at a specific operating current) can be tailored for extremely low tempcos. Known as a reference diode, this combination has seen lots of development. For tempcos below 25 ppm °C^{-1}, however, the cost becomes prohibitive for testing, matching, and selecting the diodes.

Zeners have a well-understood ageing effect, and the best reference diodes receive years of burn-in conditioning to minimize the output changes caused by ageing. Such devices are produced not by the zener manufacturers, but by specialty houses and manufacturers of high-end voltmeters and laboratory voltage standards.

The combination of a reference diode and op amp in a hybrid IC produces the amplified diode—a voltage reference with many advantages. Rather than testing and matching diodes (a procedure involving thousand of logged measurements and hundreds of parts at dozens of temperatures) you simply combine randomly selected op amps and reference diodes, and set the tempco with standard op amp trimming techniques.

Each amplified diode requires a complete temperature sweep followed by several trims, and a second temperature sweep to confirm performance, but the resulting tempco is better than 1 ppm °C^{-1}. Maxim's hybrid references, the MAX670 and MAX671, are built and tested in this way.

The MAX670/671 amplified-diode references use internal resistor networks to amplify the output to 10.000 V ±1 mV, independently of the precise zener current and voltage required for minimum tempco.

In addition, the MAX670/671's opamp is configured as a 4-wire power supply with separate force and sense leads to eliminate the effect of voltage drops along the connecting wires. As a result, the reference voltage appears exactly where it is needed—not just at the amplified-diode's output terminals (see the box on the next page). This feature is vital to low-ppm applications because it eliminates ground-loop errors, thermal voltages, and IR drops in the connections—including a socket (if used) for the voltage reference itself. (At 1 mA, a 10 mΩ trace resistance produces a 10 fV [1 ppm] error).

Kelvin connections also allow the delivery of considerable load current. If necessary, you can boost the load current to several amperes (without degrading accuracy) by adding an external pass transistor within the feedback loop. Thus, the amplified diode not only eliminates board trimming during manufacture, it ensures repeatability—both on the production line and following field repair.

The zener diode's successor is the bandgap reference. Almost impossible to make with discrete components, the bandgap reference is made practical by integrated-cir-

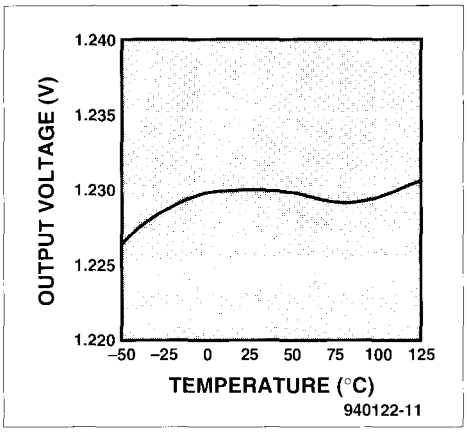


Fig. 1. The familiar 'S' curve of this bandgap reference shows a minimum variation with temperature.

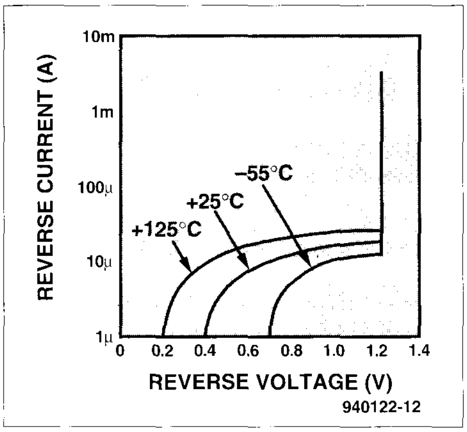


Fig. 2. Bandgap diodes have a much sharper knee than actual diodes.

Kelvin-sensed outputs

Separate force and sense paths can greatly improve the performance of a voltage reference. That arrangement (called a Kelvin connection) is common in high-accuracy designs, but it also removes most of the noise and drift in a reference circuit of modest accuracy.

Such a circuit is the 3-wire, 2.5 V reference of **Figure A**. Though suitable for use with 12-bit A/D and D/A converters, it is prone to errors that are often overlooked or dismissed as insignificant. These errors are caused almost entirely by the effects of printed-circuit resistance and poor layout.

Note, for example, that I_{ref} (10 mA) and I_{out} (100 mA) share a ground-return trace whose resistance is represented by R_5. Assuming this trace measures only 10 mΩ, the resulting direct-voltage error is 1.02 mV—nearly two LSBs in a 12-bit system with a 2.5 V reference.

Resistors R_5 and R_8 also produce variations in reference voltage as the reference load varies. These resistances may measure only 10 mΩ as printed-circuit traces, but the values (and the resulting errors) can escalate if the reference is placed in a socket, or if the reference load current passes through an edge connector. Connectors are particularly troublesome because their resistances change each time they are reconnected.

Resistors R_1 and R_3 cause less-obvious problems. They do not contribute direct voltage errors, but fast transients in the high-power load must pass through them. The resulting voltage modulation at the reference-supply pins can cause instability in the reference.

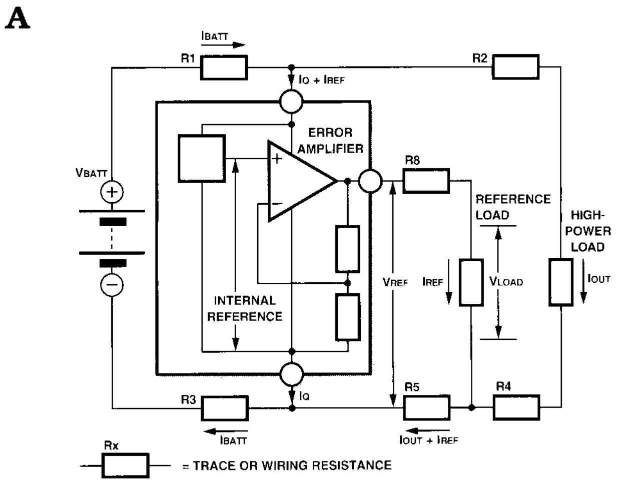
The circuitof **Figure B** is similar but offers two major improvements. First, it isolates the reference and high-power loads by providing separate paths from the high-power load all the way back to the battery terminals. High-power load transients no longer modulate the reference, because the connecting traces (R_2 and R_4) are separate from those of the reference (R_1 and R_3).

Second, the reference load is Kelvin-connected to its drive circuit. The high resistance of R_H and R_L assures accurate feedback to the error amplifier, regardless of trace resistance in the sense lines (R_7 and R_6). Moreover, the errors caused by trace resistance in the force lines (R_8 and R_5) are excluded by the amplifier's feedback (sense) connections.

Separate force and sense lines allow the reference load and its error amplifier to be separated (if necessary) by lengthy wires and numerous connectors. Calculations show that the errors in **Figure B** can be made astonishingly small—so small that little penalty accrues if you reconnect the high-power load as in **Figure A**. In that case, note that a change in the voltage across R_5 (in **Figure B**) shifts all voltages in the reference circuit, but U_{load} remains constant.

Kelvin connections not only compensate for errors that arise in passive components; they also accommodate active components such as the optional boost transistor shown in **Figure B**. With that transistor in place (replacing the R_8 force line), you can increase current-source capability in the reference without degrading accuracy. Similarly, you can increase the current-sink capability by adding a p-n-p transistor with its collector connected to ground.

Finally—the accuracy achieved with Kelvin connections eliminates the need for board trimming during manufacture. The result is repeatable performance, both for the units of a production lot and for a single unit before and after field repair.



$V_{LOAD} = V_{REF} - I_{REF} R8 - (I_{OUT} + I_{REF}) R5$

FOR 10m TRACE RESISTANCES. A 10mA REFERENCE LOAD AND A HIGH POWER LOAD, V_{LOAD} IS 1.02mV LESS THAN V_{REF}. FOR V_{REF}=2.5V, THE RESULT ERROR IS 408ppm

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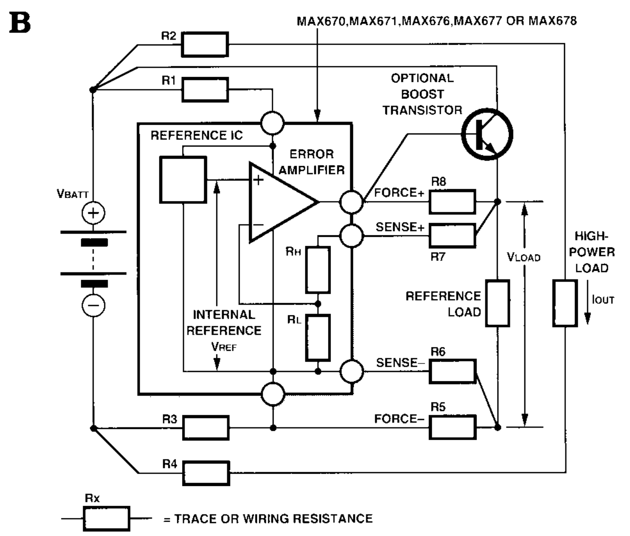


$V_{LOAD} = V_{REF} \times (R_H + R_L) / R_L \times K$

$K = (R_H+R_L+R7+R6) / (R_H+R_L) = (300{,}000+100{,}000+0.01+0.01) / (300{,}000+100{,}000) = 1.000\,000\,05$

940122-17

cuit technology. Bandgaps are based on a simple and elegant principle—take a known problem and turn it into a solution.

The problem is that forward-conducting silicon diodes have a well-defined temperature coefficient (2 mV °C^{-1}), but a hard-to-control offset voltage. The solution is to fabricate (for example) 11 identical diodes on a silicon substrate, arrayed in a tight group for close thermal matching. Connect all but one central diode in parallel. Then, drive that diode and the remaining group with two identical currents, so the central diode operates with an approximate 10-times high density across its junction. The central-diode voltage has a negative tempco, but the voltage difference (for the single diode vs the group) has positive tempco.

If you then arrange for the voltage difference (times a gain factor) plus the central-diode voltage to equal the bandgap voltage of silicon (1.205 V), the sum will (ideally) have a tempco of zero (**Figure 1**). This is what the bandgap circuit does.

The simplest and least expensive bandgap reference is a two-terminal device such as Maxim's ICL8069, which operates like a zener diode. Unlike zeners, however, the bandgap has a low voltage (1.23 V) and a very sharp knee at low operating currents: the voltage change from 50 fA to 5 mA is less than 15 mV (**Figure 2**). Low voltage and low current make bandgap references suitable for operation in feedback networks, biasing networks for opamps, and other circuits for which the zener reference is inappropriate.

Specifications

To select the best reference for a given application, you must be aware not only of the different reference types, but also of special definitions manufacturers use for the specifications that describe voltage-reference performance. The following entries define and discuss each parameter.

Accuracy. This is an ambiguous term. It is literally the sum of all deviations from the ideal output value, expressed as a fraction of the ideal, subtracted from one, and multiplied by 100. A perfect reference, therefore, is 100% accurate. But in common usage, accuracy and total error are used interchangeably. A '1%-accurate' reference is generally understood to have a total error of 1%, not 99%.

Error. A particular categeory of deviation from the ideal. Voltage-reference errors are expressed either as absolute values (mV, for instance), or as fractions, and in percent (%) or parts per million (ppm).

Initial accuracy. The output-voltage tolerance exhibited by a voltage reference following the initial turn-on of power. It is usually measured at no load or for a range of load currents. In many applications, initial accuracy is the most important specification. For low-cost references, it may be the only accuracy specification.

Turn-on drift. A change in output voltage over a specified time interval following turn-on. With or without an oven, all references exhibit some change over the first seconds or minutes following turn-on. Usually asymptotic, turn-on drift is an important specification for portable systems that conserve battery energy by powering the reference for short periods only.

Short-term drift. Similar to turn-on drift, but specified for a short period (milliseconds to minutes) at any time after turn-on. It often appears in data sheets as a chart recording or scope photo. Short-term drift differs from noise only in the units of measure; both are small, unpredictable, and random.

Long-term drift. Slow changes in voltage-reference output that occur over minutes, days, or months of continuous operation. Long-term drift, usually expressed in ppm/1000 hours, is a form of noise and is therefore random and unpredictable.

Ageing. A gradual change in output voltage caused by long-term changes in the characteristics of the reference. Ageing differs from long-term drift, however: it results in a slow unidirectional change in the reference voltage, whereas long-term drift causes random fluctuations.

Noise. Electrical noise at the output terminals of a voltage reference. It may include wideband thermal noise, low-frequency spikes of wideband (popcorn) noise, and narrow-band $1/f$ noise. Thermal noise is small and easily filtered with a simple RC network, unless the application prohibits that approach. For applications that power the reference for short intervals only, most forms of noise translate to a component of the initial accuracy.

Temperature drift. A change in output voltage caused by temperature, expressed in ppm °C^{-1} or % °C^{-1}. Usually the second most important specification after initial accuracy, it becomes dominant for applications in which the initial accuracy can be compensated by a calibration of adjustable gain. Three methods of specification are common.

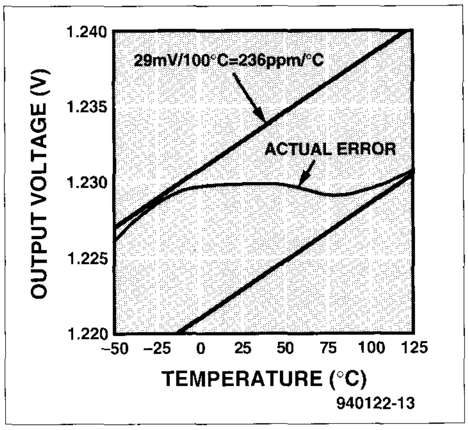


Fig. 3. The slope method of depicting U_{out} vs temperature simply illustrates the maximum dv/dt with a straight line on the graph.

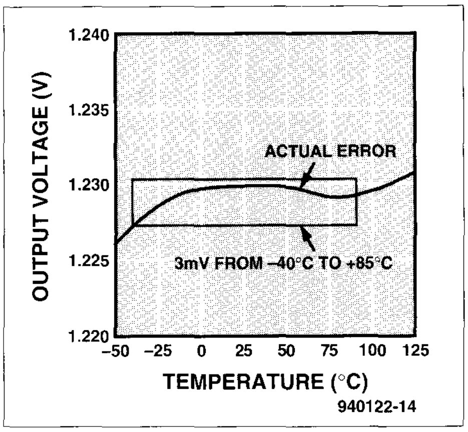


Fig. 4. The box method, which encloses the extremes of U_{out} variation within a box, gives a closer approximation to the actual error.

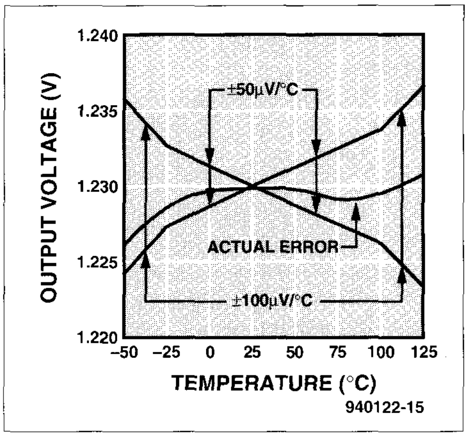


Fig. 5. The butterfly method gives one actual data point at +25 °C, plus a limiting envelope that specifies the error more tightly than does the slope method.

Slope method (**Fig. 3**): a line representing the worst-case (highest) dv/dt over the temperature range of interest. Used mostly on older military products with an assumption that the drift is linear (often wrong), this method enables worst-case calculations. One problem: the actual point of maximum slope is not specified.

Box method (**Fig. 4**): a box formed by min/max limits for output voltage over the temperature rnage of interest. This construction corresponds to the method of test, and provides a closer estimate of actual error than does the slope method. The box guarantees limits for the temperature error, but (like the slope) says nothing about the exact shape and slope of the output response.

Butterfly method (**Fig. 5**): a more detailed set of limits that actually shows one datum point (at 25 °C), with minimum and maximum slope lines passing through it, and two or more breakpoints along each line. The name comes from the shape of these lines as they appear on the graph of output voltage vs temperature.

Figures 3–5 represent the same fictitious voltage reference. Note that the numerical error estimates listed on each figure are not easily compared, but the box may be inverted by drawing a diagonal across it. That slope then allows a closer comparison with the other two methods of specification.

Self-heating. A change in temperature and consequent change in output voltage caused by the flow of load current internal to the reference. This effect is sneaky because it has several time constants ranging from microseconds to seconds. Self-heating is rarely specified because it does not appear in high-speed measurements of line and load regulation.

You can choose a reference that is specified at the extremes of load current, or eliminate self-heating by adding an external transistor or buffer amplifier to handle the load current. The monolithic, 1 ppm MAX676–MAX678 references offer another option: they include active circuitry that maintains a constant internal power dissipation as the load current changes.

Load regulation. An error produced by a change in load current. Like line regulation, this d.c. specification does not include the effects of load transients.

Line regulation. An error produced by a change in the input voltage. This d.c. specification does not include the effects of ripple voltage or line transients. For battery-powered applications, the modern voltage reference is far superior to its predecessors, both for line regulation and for the closely related specification of dropout voltage (associated with the minimum-allowed input voltage).

Dropout voltage. The minimum input-to-output voltage difference (also called minimum input-to-output differential) that will guarantee proper operation. Dropout voltage sometimes appears as a line in the specification table, but it often appears only as the lower voltage

Two-terminal and three-terminal micropower references

Two-terminal and three-terminal reference types can differ considerably in actual power consumption. Consider two circuits, each generating 2.5 V from a 6 V battery that is allowed to discharge to 3 V (see **Fig. C**).

Quiescent current for the three-terminal device is the sum of the I_Q shown in the data sheet plus the load current; this sum is fairly constant over the entire range of battery voltage. But for the two-terminal design, current is limited mainly by R_{in}, whose value is established by the minimum values for battery voltage ($V_{batt(min)}$) and quiescent current ($I_{Q(min)}$):

$$R_{in} = V_{batt(min)} - V_{ref} / (I_{Q(min)} + I_{load}).$$

For $V_{batt(min} = 3$ V and $I_{Q(min)} = 10$ fA,

$$R_{in} = (3\text{ V} - 2.5\text{ V}) / (10\text{ fA} + 100\text{ fA})$$

$$= 4545\ \Omega.$$

Over the battery's 3–6 V range,

$$I_Q + I_{batt} = (V_{batt} - V_{ref}) / R_{in}$$

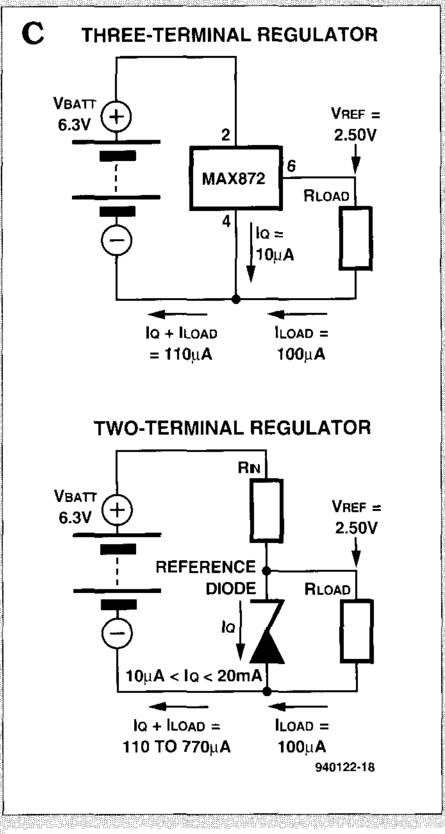
$$= 110\text{ fA for } V_{batt} = 3\text{ V},$$

and

$$= 770\text{ fA for } V_{batt} = 6\text{ V}.$$

Thus, the quiescent current can increase six-fold when you install a fresh battery.

C



Values of R_{in} less than 4545 Ω draw much more current. If, for example, you let the battery discharge to 2.7 V instead of 3 V, R_{in} becomes 1818 Ω and the battery current (at 6 V) becomes 1.925 mA. Power consumption for that condition is 11.55 mW, which is no longer micropower!

level in the conditions for the line-regulation specification. The dropout specification is particularly important for 4.096 V references powered from 5 V supplies.

Transient response is the response of a voltage-reference output to a transient of input voltage or output current. Voltage references are not power supplies, and they rarely excel in the rejection of transients. Data sheets may publish scope photos or typical curves for transient and a.c. performance, but guaranteed specifications are rare. In general, you must add other circuitry to shield the reference from line and load transients.

This review of reference types and specifications provides most of the information you will need to select a reference for your application. Also helpful are the following discussions on countering the effects of temperature, a collection of pitfalls to avoid, and another collection of hints on how to enhance the performance of your voltage reference.

Circuit pitfalls

No matter how good a reference is, poor circuit engineering can make it look bad. The following is a summary of the problems most often encountered.

Ground. Noise or offset voltage in the ground node makes all other troubleshooting measurements suspect. All measurements should be referred to the same point, which is connected to the Kelvin ground sense pin of the reference.

Noise and glitches. Use an oscilloscope to ensure that the reference output is stable. As with opamps, very high capacitive loads may cause oscillations. When monitored with a digital voltmeter, a reference output with HF oscillations appears to have very poor initial accuracy and poor stability. Also use the oscilloscope to look for transients on the reference output caused by rapidly varying load currents, such as those drawn by the reference inputs of some A/D converters.

A/D converters. These devices, particularly successive-approximation types, have high-speed switches that may introduce extremely narrow, energetic current pulses at the source and reference inputs. You may have to buffer the reference with an amplifier or a resistor of 20–100 Ω. Contrary to intuition, adding capacitance to ground can make things worse.

Buffering. The initial offset voltage, offset-voltage temperature drift, and gain errors of most buffers will significantly degrade the reference accuracy if you simply connect a buffer to the reference output. The preferred method is to include the buffer *inside* the reference's feedback loop (via its sense inputs).

Temperature. Many references include a PTAT (Proportional To Absolute Temperature) output for convenience, so you need only add (for instance) an opamp driving a power transistor in close thermal contact with the reference. As an alternative in battery-powered applications with a human operator, the PTAT voltage might drive a comparator that actuates a front-panel display, warning that the results may be out of range.

Line regulation. By filtering and pre-regulating the input voltage, a zener or three-terminal regulator can greatly improve line regulation, line-transient rejection and ripple rejection. On the other hand, most references provide only a few mA, so a simple, low-cost *RC* output filter may be appropriate.

Noise. Adding a simple *RC* lowpass filter can reduce output noise, but the capacitor should have very low ESR to be effective at the audio frequencies. Check the reference data sheet before adding capacitance to the output—too much capacitance may cause oscillation.

Source and **sink capability**. An external buffer amplifier can deliver more load current, but be sure to use a reference with separate force and sense terminals, which is designed to drive an external pass transistor within the reference's feedback loop.

Design example

A simple battery-powered adaptor (see **Fig. 6**) converts an ordinary DVM into a 4-wire milliohmmeter that accurately measures the resistance of wiring, motor coils, solenoids,high-current inductors, and meter shunts. It can quickly locate short-circuits in a power supply or on a printed-circuit board. The circuit shown is about 2% accurate. For higher accuracy, you can make component adustments as described below.

The circuit applies 1 A, 100 mA, or 10 mA, according to to the range switch setting, to the unknown resistance via two test leads. You then set a DVM to the 2 V range and connect it with two more test leads, forming a 4-wire connection to the resistance being measured.

The DVM indicates directly in ohms when you depress the momentary-on power switch, S_1. A 1000 Ω resistance, for instance, reads 1.000 V on the circuit's 1 A range, so 1 mV corresponds to 1 mΩ. Four-digit and five-digit DVMs frequently have 1 µV sensitivity, providing resolutions of 1 µΩ. Because the output is a current source, the

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unknown resistance of the connections and test leads is not a source of measurement error.

Accuracy depends on the DVM, the op amp's input offset voltage (±70 µV max), and the tolerance of R_1, R_2, R_4, R_5, and R_6. First, trim the 1 A range by selecting R_4 or by adding a trimming potentiometer between R_1 and R_2. Next, trim the 100 mA range and then the 10 mA range by adjusting the highest-valued resistors in the R_5 and R_6 networks.

Depressing S_1 turns on the micropower reference, IC_1, which produces 2.500 V. Resistors R_1 and R_2 divide that output to 0.1 V, and the op amp forces 0.1 V at the source of T_1. This action creates a current source that develops 0.1 V across R_4, R_5 and R_6. The range switch selects a current of 1 A, 100 mA or 10 mA in the loop formed by the resistors, the unknown resistance, the 1.5 V battery, and T_1.

Note that releasing S_1 (or disconnecting the adaptor) eliminates all current drain from the 1.5 V battery. An alkaline D cell therefore produces thousands of measurements, even on the 1 A range, if you depress S_1 for brief readings on the DVM only. The 9 V battery can last for years because its load is smaller than 30 µA.

To search for a short-circuited component or a short between tracks on a PCB, first connect the two adaptor leads, one to each of the relevant tracks. Connect a DVM lead to the same point as one adaptor lead, and use the other DVM lead to probe along the tracks. The highest reading on one track and the lowest reading on the other track reveal the location of the short-circuit. Constant readings indicate no adaptor current flowing in that section of the track (for a given connection of the adaptor leads), so you can eliminate that section from the search. [940122]

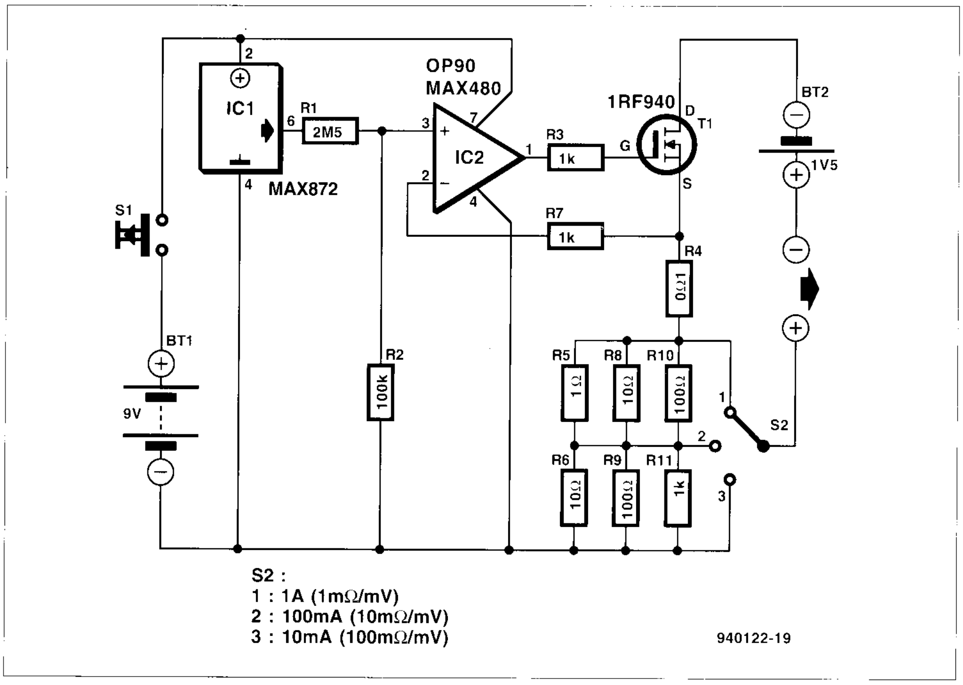

Fig. 6. Operating with a DVM, this low-power adaptor circuit performs 4-wire, low-resistance measurements.

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This little book covers roughly the same grounds as the PIC programming course featured in four instalments in *Elektor Electronics* last year, although it must be noted that its entrance level is much lower. The title of Mr. Gardner's book is, therefore, fully appropriate, because the 'Beginners Guide' is excellent for those who have never worked with Microchip Technologies' PIC series of RISC microcontrollers.

The book lays a solid base by first discussing elementary concepts such as ASCII and hexadecimal notation, file formats and product development, before discussing the internal structure of the PIC. Then comes the interesting bit: hardware interfacing and programming. A good discussion is presented on the choice of oscillators for the PIC, which is an important setting before any programming can be done.

The MSDOS diskette supplied with the book contains the well-known Microchip PIC assembler, MPALC, and the associated simulator, as well as source code listings of the programs discussed in the book. Very useful if you do not like typing!

The book contains references to manufacturers of PIC related products such as programmers and starter kits. Unfortunately, this book was published just before the *Elektor Electronics* 'PIC programmer' article.

The sections on debugging are partly original, and partly reproduced from an earlier publication in *Electronic Design*. Although concise, they provide enough information to eleminate the majority of problems which may arise during PIC program development.

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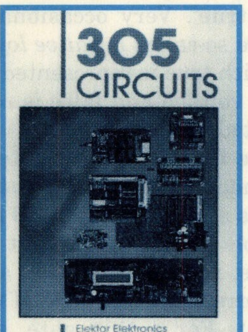

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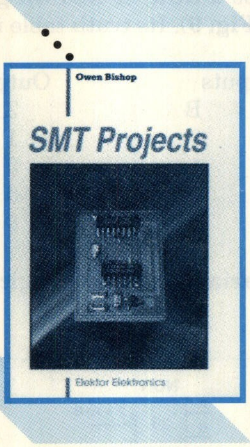

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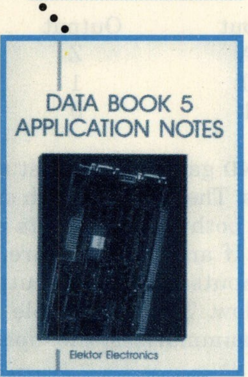

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THE DIGITAL SOLUTION

Part 2 – Digital essentials

By Owen Bishop

In this series we look closely at digital electronics, what it is, what it does, how it works, and its promise for the future.

Before we go on to examine digital circuits in detail, we will run briefly through some of the essential background to an understanding of digital electronics. Last month we explained the binary basis of digital circuits and how facts and numbers can be represented in them. We also described the three fundamental logic operators: NOT, AND and OR.

Circuits can be built to perform the function of a logic operator. Such a circuit is known as a *logic gate*. A gate has one or more inputs, but only one output. It is possible to assemble gates from discrete components, such as transistors, diodes and resistors, but this ia rarely done. Almost invariably we use an integrated circuit that provides one or (usually) more gates. **Figure 5** shows a typical logic IC: the symbols drawn within the outline show the pin connections of the six identical gates it contains. Each gate performs the NOT operation. Two pins provide the power connections to all six gates. Each gate has one input and one output. The symbol used in logic diagrams for a NOT gate is a rectangle with a figure 1 inside and a short slanting stroke at the output. It is the slanting stroke that indicates the inverse nature of the output.

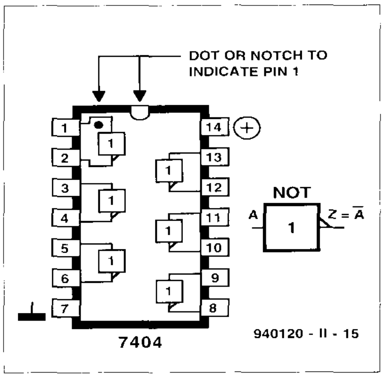

Fig. 5.

A NOT gate may be in one of two states:

U_{in} high → U_{out} low

U_{in} low → U_{out} high.

The output is the inverse (or complement) of the input. If we take a high input or output to represent 'true', a low input or output represents 'false' or 'NOT true'. Very occasionally we use so-called *negative logic*, in which true is represented by a low voltage and false is represented by a high voltage.

The behaviour of a gate is summed up in a *truth table*. This is a table that lists all the possible states of the input (or inputs, if more than one) and the corresponding states of the output. For a NOT gate, the truth table is

Input	Output
A	Z
0	1
1	0

An AND gate has at least two inputs. The output is high only when both (or all) inputs are high. If any one, or more, of the inputs is low, the output goes low. The truth table for AND summarizes the operation:

Inputs		Output
A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1

Note that the four lines of the table cover all four possible combinations of states of the two inputs. A three-input AND gate has this truth table:

	Inputs		Output
A	B	C	Z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Z is true only when A AND B AND C are true. Once again we have covered all possible combinations of inputs. Note that the way to ensure that all possibilities are listed is to fill columns A to C with the binary numbers equivalent to 0 to 7. **Figure 6** shows the commonly used symbols for 2-input and 3-input AND gates.

A high input on any one or more inputs of an OR gate gives a high output. The truth table for a 2-input NOR gate is:

Inputs		Output
A	B	Z
0	0	0
0	1	1
1	0	1
1	1	1

Compare this with the truth table for an AND gate. **Figure 7** shows the symbols for the 2-input and 3-input OR gates.

Although OR, AND, and NOT gates are able to cover all possible logic operations, a particular circuit may require a large number of such gates. Simplification and reduction in gate numbers is made possible by the use of certain other types of gate.

Figure 8 shows the symbol for a NAND gate. As the symbol implies, this is an AND gate with a negated output. Its logic equivalent in terms of AND and NOT is shown in **Fig. 8b**. Its name is a contraction of NOT-AND. Note that the negation of AB (or NOT-AB) is indicated by a bar over AB to give $\overline{AB}$. Here is the truth table for a 2-input NAND gate:

Inputs		Output
A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

Corresponding to NAND, there is also a NOR, or NOT-OR gate (see **Fig. 9**). Its truth table is:

Inputs		Output
A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0

A variation of OR logic is

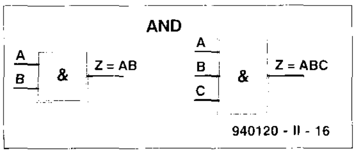

Fig. 6.

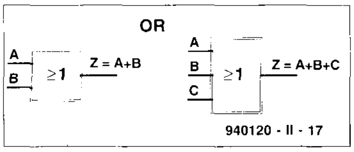

Fig. 7.

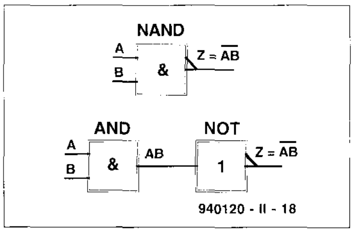

Fig. 8.

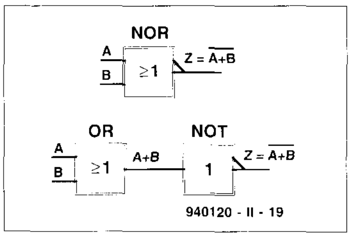

Fig. 9.

known as exclusive OR or XOR. It applies only to a 2-input gate. The output of an OR gate is high if one input or the other or *both* inputs are high. The output of an XOR gate is high if one input or the other, but NOT both, is high. This is shown in the truth table:

Inputs		Output
A	B	Z
0	0	0
0	1	1
1	0	1
1	1	0

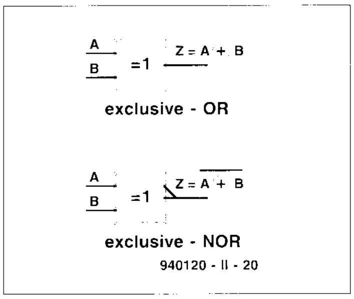

Fig. 10.

There is also an exclusive-NOT gate whose output is the inverse of an XOR gate. The XNOR gate is also known as the *parity gate* or *coincidence gate*, since its output is high when both inputs are low or both are high. The symbols for XOR and XNOR gates are shown in **Fig. 10**.

All logic operations can be performed with only NAND gates or only NOR gates as will be explained later.

Logic families

There are several ways of implementing a gate as an integrated circuit. Manufacturers have produced several families of ICs that comprise not only individual logic gates but also more complicated logic circuits consisting of several or many such gates connected together on a single chip. The more complex logic devices include counters, dividers, coders and decoders, registers, and arithmetic units. The most complex of all include microprocessors, memories, modems and many other specialized logic devices. A family of logic ICs is based on one particular method of fabrication. One of the most successful and widely used of these is *transistor-transistor logic*, abbreviated to TTL. The circuit of a gate is based on a number of n-p-n bipolar transistors plus a few resistors and diodes. The ICs of this series all have a type number beginning with 74. This is followed by two or more digits to indicate the device or devices in the IC. For example, 7400 has four 2-input NAND gates; 7404 has six NOT gates; 74151 is a more complex IC, an 8-bit multiplexer or data selector.

The 74 series is used less often nowadays, since it has been superseded by several variants, identified by code letters in the type number. The performance of these sub-families is superior to that of the original 74 series in various ways. Thus, the 74LS series requires less power. The 74HC series is based on complementary MOS transistors; its power requirement is very small and it has a wider range of operating voltages. In particular, it can operate on voltages as low as 2 V, making it very suitable for battery-powered equipment. The 74AC series is able to operate at higher speed than the other series. All series have equivalent ICs; for example, the 74LS00, 74HC00 and 74AC00 all have four 2-input NAND gates with identical pin connections.

Another major series is the 4000 series. This has ICs that are equivalent to the 7400 series. For example, the 4011, with four 2-input NAND gates, is the equivalent of the 7400, though the pin connections are slightly different. The 4000 series has a wide range of operating voltages (3-15 V), but is appreciably slower than the 7400 series and its relatives. But it is fast enough for many purposes.

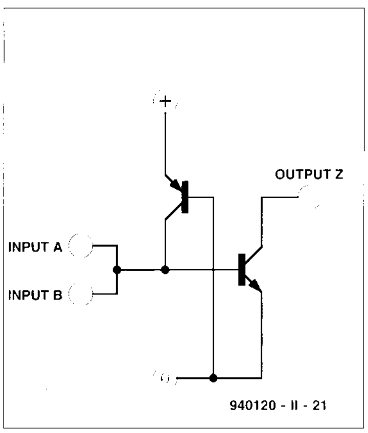

Fig. 11.

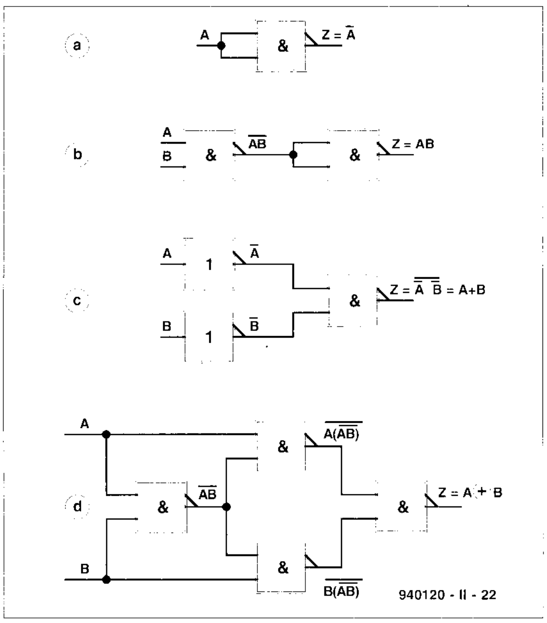
a
A
&
Z = Ā
b
A
B
&
$\overline{AB}$
&
Z = AB
c
A
1
Ā
B
1
B̄
&
Z = $\overline{\bar{A}\ \bar{B}}$ = A+B
d
A
&
$\overline{AB}$
&
$\overline{A(\overline{AB})}$
&
Z = A ⊕ B
B
&
$\overline{B(\overline{AB})}$
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Fig. 12.

Emitter-coupled logic (ECL) is one of the fastest families. Its speed is due to the bipolar transistors not being switched fully on. This means that they are not saturated and it takes far less time to switch them off again. The disadvantage is that high and low levels are close and ECL is relatively more subject to noise.

Integrated injection logic (I^2L) has a very simple construction (see **Fig. 11**), with no on-chip resistors. This results in considerable saving of space, so making I^2L particularly suitable for building highly complex circuits on a single chip. In the NAND gate of **Fig. 11**, a low input to either one or both of the input terminals draws current through the p-n-p transistor and turns the n-p-n transistor off. This gives a high-impedance output, that is, one which draws no current from the input of an I^2L gate connected to it. If both inputs are high, current flows to the base of the n-p-n transistor, turning it on. The output will now draw current from another gate input, so it acts as a low-impedance output. The demand for fast low-power ICs for use in battery-powered equipment such as lap-top computers has led to the development of low-voltage CMOS ICs. Series such as LV-HCMOS and HLL operate on 3.3 V.

Logic operations

It was stated earlier that all logic operations can be performed with nothing but NAND gates or NOR gates. **Figure 12** shows how the basic operations may be performed. In **Fig. 12a** the inputs of the NAND gate are wired together, so they are both high or both low. Examination of the truth

	(a) AND gate	**(b) OR gate**	**(c) NOT gate**
1	AB = BA	A+B = B+A	
2	(AB)C = A(BC)	(A+B)+C = = A+(B+C)	
3	AA = A	A+A = A	
4	A·1 = A	A+1 = 1	
5	A0 = 0	A+0 = A	
6	A(B+C)	AB+AC	
7	ĀA = 0	A+Ā = 1	
8			A = A

Box 3. The eight theorems derived from the basic rules of Boolean Algebra.

table for NAND shows that only the first and last lines apply, giving the same table as that for NOT. In **Fig. 12b**, we use this action to invert the action of a NAND gate and so obtain AND.

The action of the circuit of **Fig. 12c** is best followed by using a truth table. We use this as an example of the techniques used for symbolizing logic operations.

A	B	$\overline{A}$	$\overline{B}$	$\overline{A}\,\overline{B}$	$\overline{\overline{A}\,\overline{B}}$
0	0	1	1	1	0
0	1	1	0	0	1
1	0	0	1	0	1
1	1	0	0	0	1

Begin by filling in all possible combinations of inputs in the first pair of columns. In the second pair of columns, we have the outputs of the NOT gates, which consist of the inverse of their inputs. That these are inverses is indicated by the bar over each symbol. In the column headed $\overline{A}\,\overline{B}$, we have the effect of ANDing $\overline{A}$ and $\overline{B}$ (check with the truth table for AND that values are entered correctly). This is the first stage of the NAND operation. To symbolize the AND operation, it is conventional to write the symbols A and B side by side with no gap between them, just as when we write *ab* in algebra to indicate multiplying *a* by *b*. In the last column we have the inverse of $\overline{A}\,\overline{B}$, written $\overline{\overline{A}\,\overline{B}}$. This completes the NAND operation. Comparing the last column with the truth table for OR, we see that they are identical: NANDing the inverses of A and B is the same as ORing them.

Figure 12d shows how to build an XOR gate from NAND gates. The truth table is:

A	B	$\overline{AB}$	$\overline{A(\overline{AB})}$	$\overline{B(\overline{AB})}$	A⊕B
0	0	1	1	1	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	1	1	0

Use the table for NAND to work out the steps in the table above. In the last column we write the NAND of the two previous columns. Comparison with the table for XOR shows that these four NAND gates perform the function of XOR. The last column is headed with A and B joined by the symbol for XOR. The symbol for XOR is ⊕ and that for XNOR is Θ.

These few examples show that electronic circuits are able to perform a range of logic operations from the simplest to the most complex.

Boolean algebra

It is clear from the preceding section that there is more than one way to effect a logic operation. One of the aims of logic circuit design is to reduce the number of gates required to a minimum. Logic expressions can be simplified according to the rules of Boolean Algebra. The basic rules, or axioms, are those which govern the operation of NOT, AND and OR gates. From these we derive a number of theorems which are listed in **Box 3**. A and B are logic variables that can take the value 1 (high) or 0 (low). In the box, the symbol · represents AND, where writing the two symbols side by side would not be clear. To confirm any of the eight theorems, draw out the corresponding logic diagram and consult the appropriate truth tables. Theorems 1, 2 and 6 can be extended to apply to a greater number of variables.

Simplifying logic diagrams is a matter of using the theorems. Take the diagram in **Fig. 13** as an example. Start by labelling the inputs A, B and C. Work from left to right, writing the output values against each gate and carrying these values on to the next gate. The result is the equation:

$$Z = AB(B+\overline{A}C).$$

Removing the brackets (Theorem 6a):

$$Z = ABB+AB\overline{A}C.$$

But BB = B (Theorem 3a), and AA = 0 (Theorem 7a):

$$Z = AB+0\cdot BC.$$

From Theorem 5a:

$$Z = AB+0.$$

From Theorem 5b:

$$Z = AB.$$

Thus, the circuit of five gates simplifies to just one AND gate. Also, the result shows that the value of Z does not depend on the value of C. Not all circuits will reduce so dramatically, but it is usually possible to make at least a small reduction in the number of gates. One useful technique for analysing and then simplifying logic statements is a *Karnaugh Map*. This is really a different way of setting out the truth table for the number of variables involved, followed by a routine for simplifying the expressions and for identifying redundant variables (such as C in the example above). For details of the Karnaugh technique, the reader is referred to one of the standard textbooks on Boolean algebra.

Digital maths

Electronic circuits can handle logic and, since maths has a very logical basis, they have no difficulty in handling numerical operations, too. The only condition is that the numbers must be expressed in the binary system. Let us look at binary addition. The rules for adding two binary digits are

0+0 = 0
0+1 = 1
1+0 = 1
1+1 = 1, carry 1.

Ignoring the carry for the moment, we can set out the digits to be added (A and B) and their sum (Z) in a table:

A	B	Z
0	0	0
0	1	1
1	0	1
1	1	0

This is recognizable at a glance as the truth table for XOR. One stage, at least, of binary addition can be done with one of the logic gates we have already described. The table for the carry digit, Z', is:

A	B	Z'
0	0	0
0	1	0
1	0	0
1	1	1

This is the truth table for AND. Since we need an AND gate for the carry digit, we do not need an XOR gate as such; the combination of AND and two NORs in **Fig. 14** performs the XOR function. This circuit is known as a *half-adder*, because its operation is restricted to adding two one-digit binary numbers.

Sometimes, this is all that is required, but more often we want to add two numbers which each have several digits. For this operation we need a circuit that is able to accept the carry-in digit from a previous stage of addition. **Figure 15** shows the circuit of a *full-adder*, which has an input for the carry-in digit. Its outputs are Z (the sum of A, B, and the carry-in digit), and a carry-out, Z', to the next stage.

To add two binary numbers of *n* digits each, we need a half-adder for the first digit and (*n*–1) full-adders for the other digits (**Fig. 16**). Such a circuit is able to add all the digits of the two numbers simultaneously and is known as

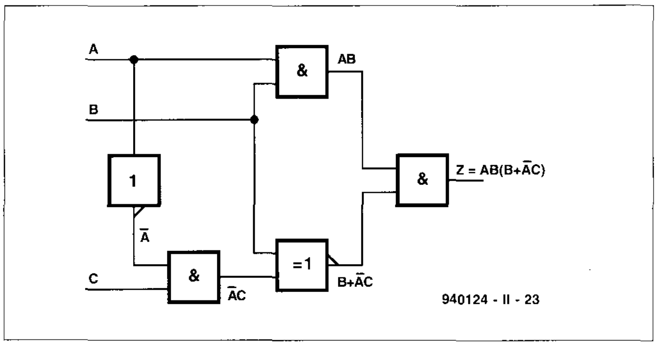

Fig. 13.

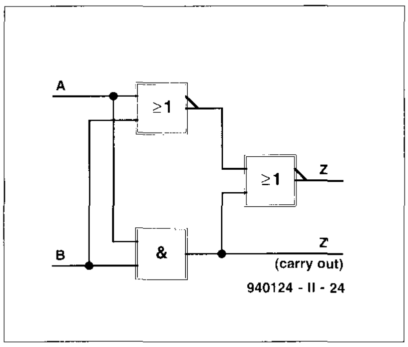

Fig. 14.

a *parallel adder*. In practice, addition is not completely simultaneous, for it takes time for each stage to produce the carry digit and pass it on to the next stage. The carry process *ripples* along the chain of adders and, until carrying has reached the last adder of the chain, the output will be incorrect. This ripple effect is something that has to be taken account of in the design of digital circuits.

Binary subtraction

It is possible to design logic circuits to subtract one binary number from another, but there is no need to go to such lengths. With a little manipulation of the digits, we can arrange for them to be subtracted by using an addition circuit. There are two methods, the first of which uses the *1's complement*. This is obtained by writing (or obtaining by a NOT gate) the inverse of each digit of the number to be subtracted. For example, find

100101–11001.

The 1's complement of 11001 is 00110

Add 100101

Sum 101011

Remove the digit from the left of the sum and add it to the remainder

01011

1

Result 1100

This technique is easily performed by logic circuits or a computer program. Another technique uses the *2's complement*. This is obtained by taking the 1's complement and additing 1 to it. In the example above, the 2's complement of 11001 is

00110

Add 1

Gives 00111

Add 100101

Sum 101100

Remove the digit from the left and discard it; the result is 01100 = 1100 since the 0 at the left can be ignored. Most computers use the 2's complement.

Negative numbers

Sometimes we use a special convention for expressing negative numbers. The first digit (or binary digit or bit) is used as a *sign bit*. If this is 0, the number is positive; if it is 1, the number is negative. The rest of the number represents its magnitude. If the sign bit is 0 (positive number), the remaining bit represents the magnitude in the usual way. If the sign bit is 1 (negative number), the remaining bits represent the 1's complement or the 2's complement. Using this system, we add the sign bits along with the rest of the numbers so the same logic circuit is used, whether or not the sign bit convention is used. If two positive numbers are added, the result is the same in either case. If one or both are negative, we need to take the convention into account when interpreting the result. In the example above, which may be rewritten as 100101+(–11001), write the numbers according to the sign bit convention, noting that both numbers must have the same number of digits: +100101 is written 0100101; –11001 is first written as –011001 to give it the same number of digits, then takes its complement. The 2's complement is 100101+1 = 100111. Precede by the negative sign bit to obtain 1100111 and add the two numbers:

0100101

+ 1100111

Sum 10001100

As usual in 2's complement arithmetic, discard the first digit to give 0001100. This begins with a 0, so it is positive with a value 001100 = 1100.

Subtracting the first number from the second: 11001+(–100101) gives a negative result: write 11001 as 0011001, including the sign bit and 100101 as its 2's complement, preceded by its negative sign bit: 1011011. Thus

0011001

+ 1011011

gives 1110100.

The first digit shows that the result is negative. The 2's complement of the remainder is 001011+1 = 001100 = 1100.

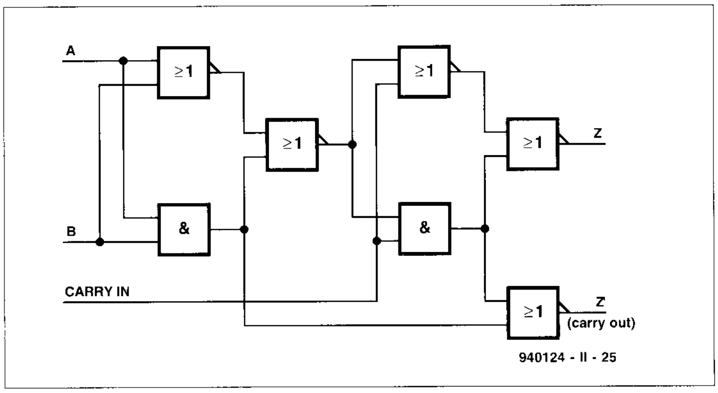

Fig. 15.

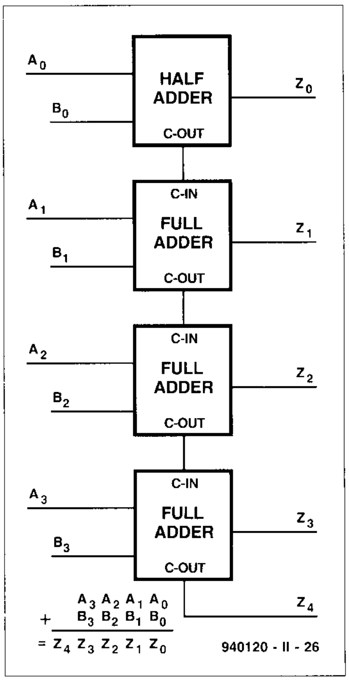

Fig. 16.

Next month we shall see how this outline of essentials is applied in practice.

Test yourself

1. Show by writing out the truth table that inverting A and B and then ORing them is equivalent to ANDing them.
2. Check that the circuit of **Fig. 14** adds correctly by writing out its truth tables.
3. Find:
   (a) 11001011+1001101;
   (b) 10101010–111101.

Answers to Test yourself (1)

1. a) 10011; b) 101101; c) 10100111.
2. a) 12; b) 39; c) 2897.
3. a) 16; b) 5F; c) CD7.
4. 011010000010.
5. 951.

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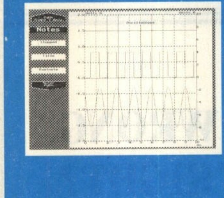

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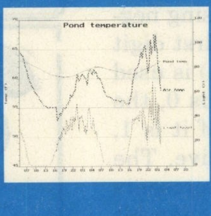

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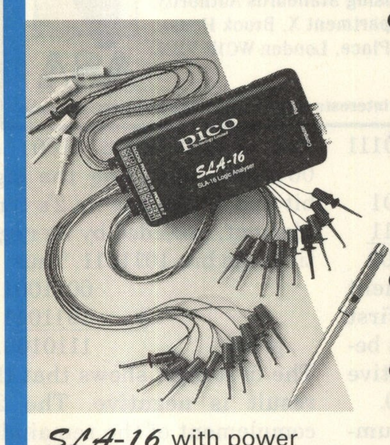

- **Connects to PC serial port, ideal for desktops or notebooks.**
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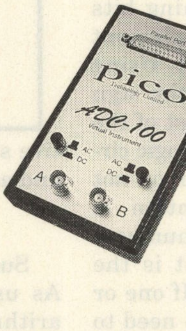
SLA-16 with power supply and cables **£219**

NEW *ADC-100* Virtual Instrument

Dual Channel 12 bit resolution



- **Digital Storage Scope**
- **Spectrum Analyser**
- **Frequency Meter**
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The ADC-100 offers both a high sampling rate (100kHz) and a high resolution. It is ideal as a general purpose test instrument either in the lab or in the field. Flexible input ranges (±200mV to ±20V) allows the unit to connect directly to a wide variety of signals.

ADC-100 with PicoScope **£199**
with PicoScope & PicoLog **£209**

ADC-10

1 Channel 8 bit

- Lowest cost
- Up to 22kHz sampling
- 0 -5V input range

The ADC-10 gives your computer a single channel of analog input. Simply plug into the parallel port and your ready to go.

ADC-10 with PicoScope **£49**

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11 Channel 10 bit

- Digital output
- Up to 18kHz sampling
- 0 -2.5V input range

The ADC-11 provides 11 channels of analog input in a case slightly larger than a matchbox. It is ideal for portable data logging using a "notebook" computer.

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1 Channel 12 bit

- High resolution
- Up to 17kHz sampling
- 0 -5V input range

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8 Channel 16 bit+sign

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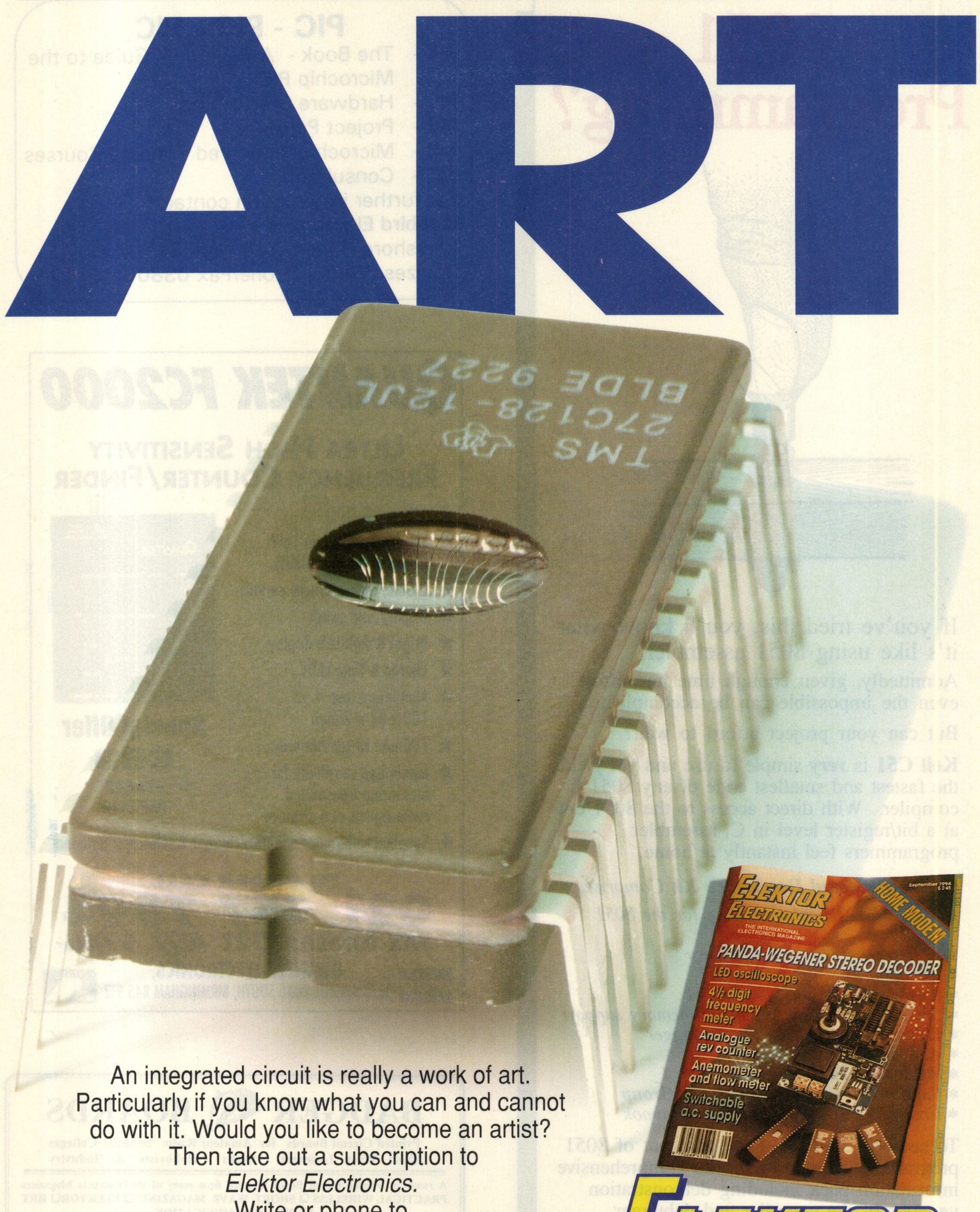

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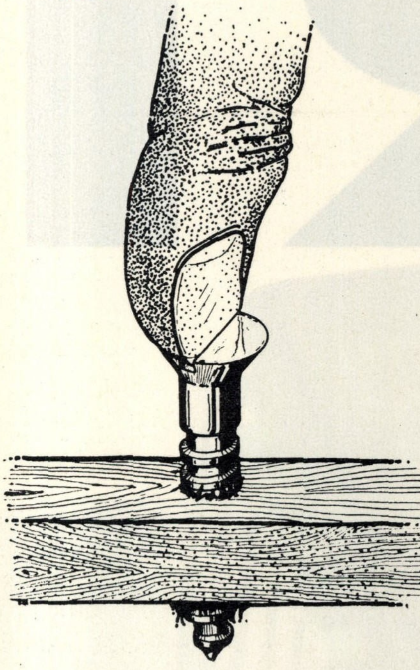
8051 Programming?



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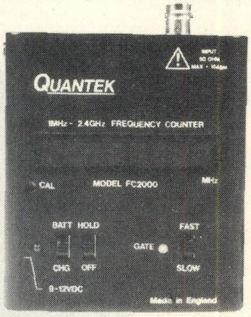

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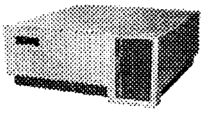

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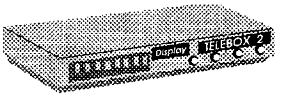

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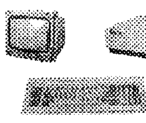

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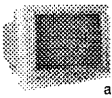

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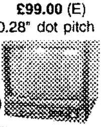

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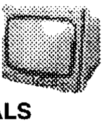

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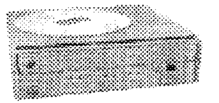

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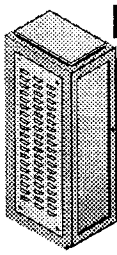

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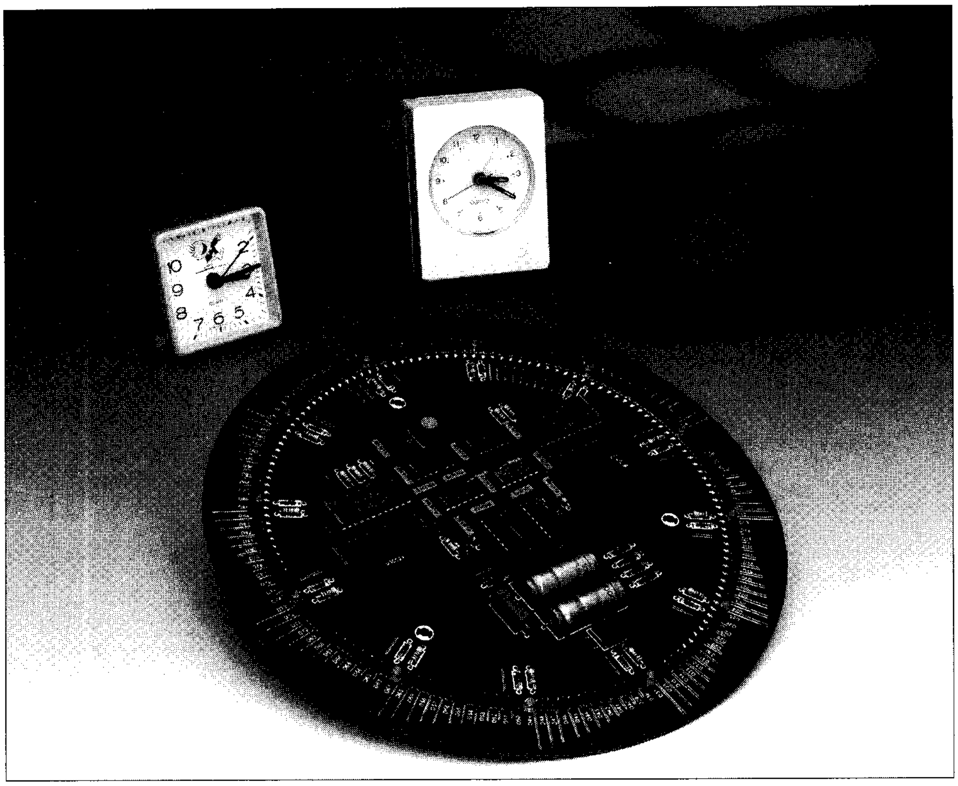
QUASI-ANALOGUE CLOCKWORK

Digital watches with displays consisting of numbers only have lost much of their popularity over the last few years. They are now outnumbered by traditional dials with hour and minute hands actuated by a digitally controlled stepper motor. These watches (and clocks) are the best of both worlds because they have an analogue readout with digital control. The LED clock described in this article is based on the same principle, only there are no moving parts at all.



Design by P. Hogenkamp

THE quasi-analogue clockwork discussed in this article uses 144 LEDs (light emitting diodes) to indicate the time on a round, quasi-analogue dial with a diameter of about 22cm. One of twelve green LEDs lights at maximum intensity to mark the hours, while the other eleven are dimmed. Between two green LEDs sit 11 red LEDs, each of which represents a period of five minutes. In this way, the time is indicated with an accuracy of five minutes. This would seem to be enough in view of the mostly decorative function of the present clockwork.

To keep the circuit as simple as possible, it is based on discrete logic integrated circuits from the 4000 CMOS series only.

Circuit description

The complete circuit diagram of the clockwork is given in **Fig. 1**. The power supply is a simple, conventional, design which also supplies a pulse-shaped 50-Hz signal. These pulses are derived from the mains voltage with the aid of a network consisting of R_{20} and C_5. Next, Schmitt-trigger IC_{4b} turns the sine-wave shaped pulses into rectangular pulses which are used to clock counter/divider IC_1. Since this IC is wired for a total divisor is 1,500, the frequency of the output signal is 1/300 Hz. That equals one pulse per five minutes. A divisor of 1,500 is achieved by detecting the binary code '1500' with the aid of IC_{2a} and IC_{2b}. When the value 1500 is reached, a pulse is generated via R_5 and C_1. The pulse is cleaned and shaped by gates IC_{3c} and IC_{3d}. Next, it resets IC_1, and increases the contents of IC_5 by one. The other input of IC_{3d} is connected to push button S_1. This button serves to adjust the clock. The pulse supplied by the push-button is 'debounced' by network R_3-R_2-C_3. Every time the button is pressed, the readout will advance by one LED position.

Circuit IC_5 operates as a five-minutes counter, and has 12 states, corresponding to 0, 5, 10, 15, 20, 25, 30, 35, 40, 45, 50 and 55 minutes.The outputs of IC_5 determine which output of multiplexer IC_7 (a 4067) is actuated. The common input of the multiplexer is connected to the +12 V supply rail via a 680-Ω resistor, R_1. When all multiplexer inputs (A-D) are held at 0, the anode terminals of the LEDs connected to output A0 (D_1, D_{13}, D_{25}, D_{37}, D_{49}, D_{61}, D_{73}, D_{85}, D_{97}, D_{109}, D_{121} and D_{133}) are connected to the 12-V supply via resistor R_1. To make a LED light, however, its cathode must be pulled to ground. That is done by another multiplexer, IC_8, which has its common output connected to ground via R_4 (820 Ω). The binary pattern applied to the A-D inputs determines which LED has its cathode connected to ground.

As soon as IC_5 reaches state '12' (which corresponds to 0 minutes), the counter is reset via IC_{4c} and IC_{4d}. Also, IC_6 receives a clock pulse which marks the start of a new hour. Increasing the contents of IC_6 results in the next output of IC_8 going low. The multiplexer then ensures that the cathodes of the selected LEDs are pulled to ground. As soon as IC_6 supplies the binary code '12', a reset pulse is generated via IC_{3b}, R_7, C_4 and IC_{3a}. This pulse resets IC_6 to state '0', so that the counter can start to count 12 hours again.

The structure of the LED matrix may be a bit difficult to distill from the circuit diagram. It is, therefore, shown separately in **Fig. 2**.

As already mentioned, the display has 132 red LEDs and 12 green LEDs. The green LEDs light continuously at low intensity. This is achieved by connecting their cathodes to ground via 10-kΩ resistors (R_8-R_{19}). If you want to increase the brightness of the green LEDs, you may lower the value of R_8-R_{19} to, for instance, 3.3 kΩ. Since the anodes of the LEDs are connected to +12 V via resistor R_{23}, a constant current of about 0.5 mA flows through each LED. At the full hour, the relevant green LED must light at maxi-

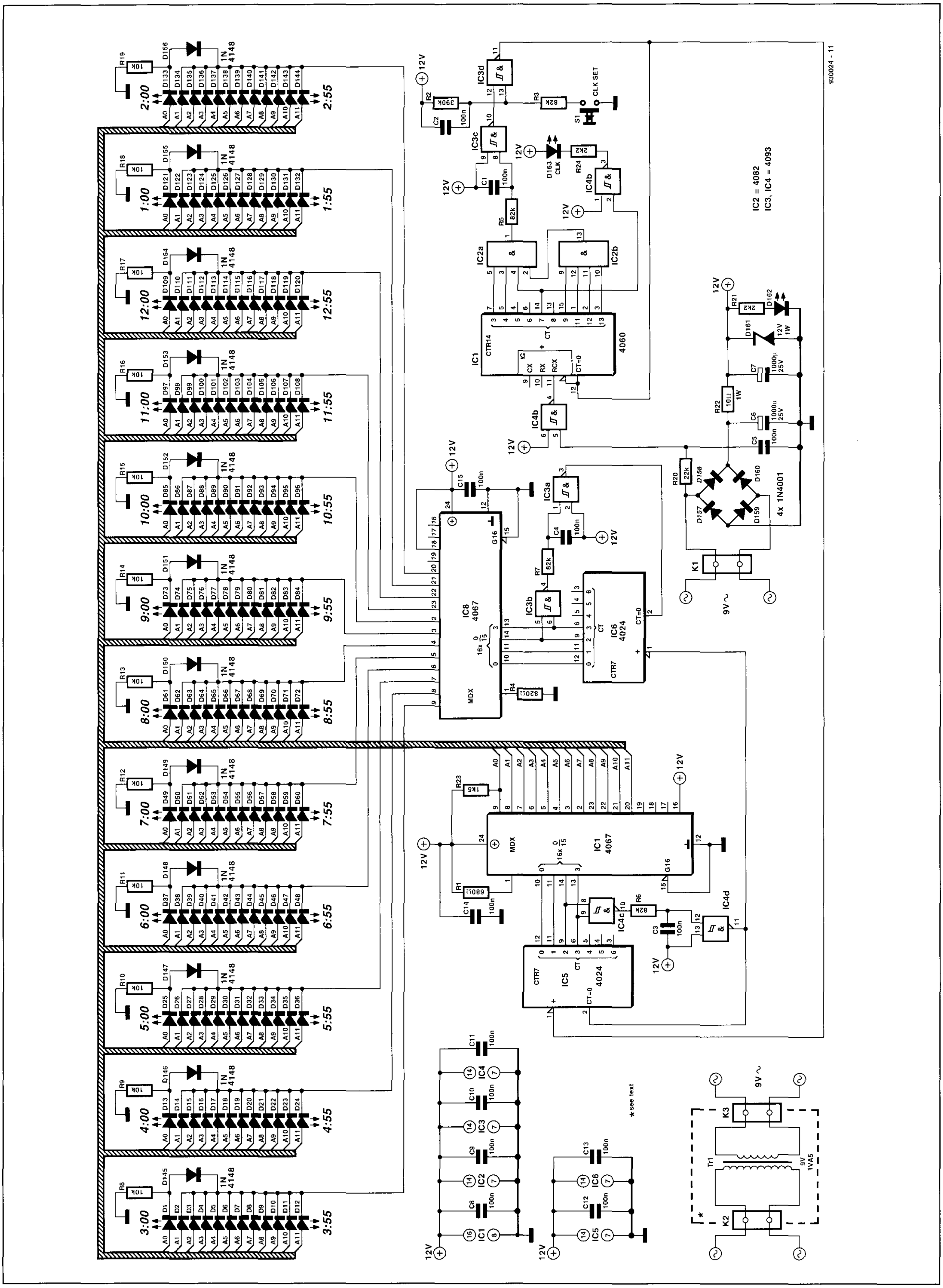


Fig. 1. Circuit diagram of the quasi-analogue clockwork.

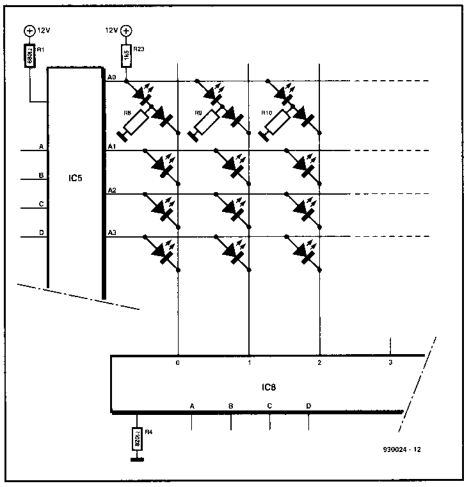


Fig. 2. Schematic structure of the LED matrix. Note that the LEDs which indicate the hours are connected in a special way.

mum intensity. That is achieved by connecting a diode and an 820-Ω resistor, R_4, in parallel with the selected LED. This trick explains why the LEDs connected to line A0 are wired differently in the matrix.

The power supply of the clockwork is straightforward. A discrete bridge rectifier turns the 9-V alternating voltage applied by a transformer into a direct voltage of about 12.5 V. A resistor-zener diode stabilizer, R_{22}-D_{161}, is used to obtain a reasonably stable +12 V supply voltage. LED D_{162} is located in the centre of the dial, and lights as a soon as the supply voltage is present. The last LED on the dial, D_{163}, flashes at a slow rate to indicate that the clock is 'ticking'.

Construction

The printed circuit board designed for the clockwork has a fairly unusual size and shape. The special design is necessary because the circuit board doubles as the dial of the clock. The track layout and component mounting plan

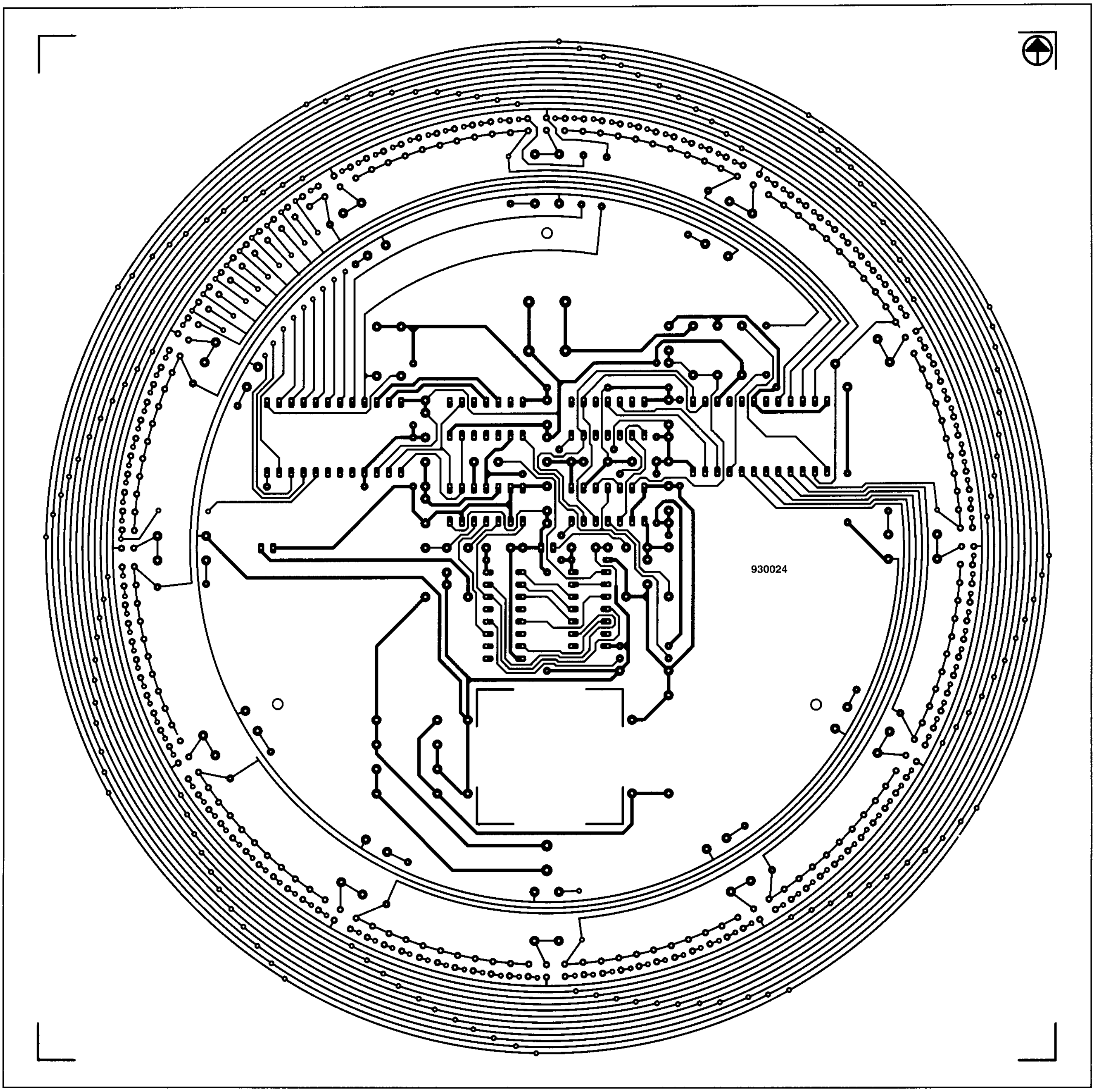


Fig. 3. Track layout and component mounting plan of the clockwork PCB, shown at 85% of true size (board available ready-made through the

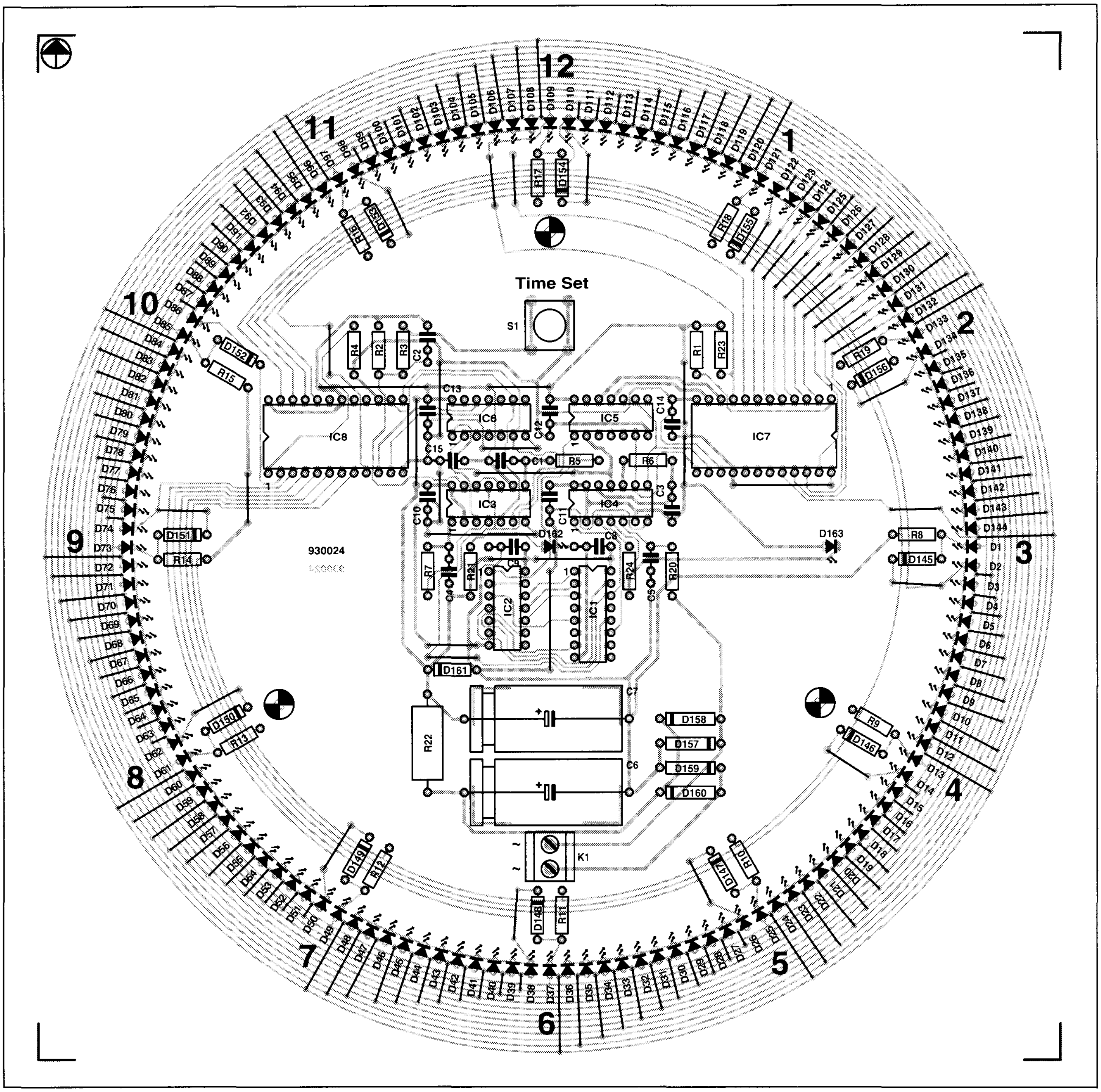
COMPONENTS LIST

Resistors:
R1 = 680Ω
R2 = 390kΩ
R3;R5;R6;R7 = 82kΩ
R8-R19 = 10kΩ
R20 = 22kΩ
R21;R24 = 2kΩ2
R22 = 10Ω 1W
R23 = 1kΩ5

Capacitors:
C1-C5;C8-C15 = 100nF
C6;C7 = 100μF 25V

Semiconductors:
D1;D13;D25;D37;D49;D61;D73;D85;D97;D109;D121;D133 = LED, green, 3mm
D2-D12;D14-D24;D26-D36;D38-D48;D50-D60;D62-D72;D74-D84;D86-D96;D98-D108;D110-D120;D122-D132;D134-D144;D162;D163 = LED, red, 3mm
D145-D156 = 1N4148
D157-D160 = 1N4001
D161 = 12V 1W zener diode
IC1 = 4060
IC2 = 4082
IC3;IC4 = 4093
IC5;IC6 = 4024
IC7;IC8 = 4067

Miscellaneous:
K1;K3 = 2-way PCB terminal block, raster 5mm
K2 = 2-way PCB terminal block, raster 7.5mm
S1 = Multimec 2CTL2 press key.
Printed circuit board 930024 (see page 78).



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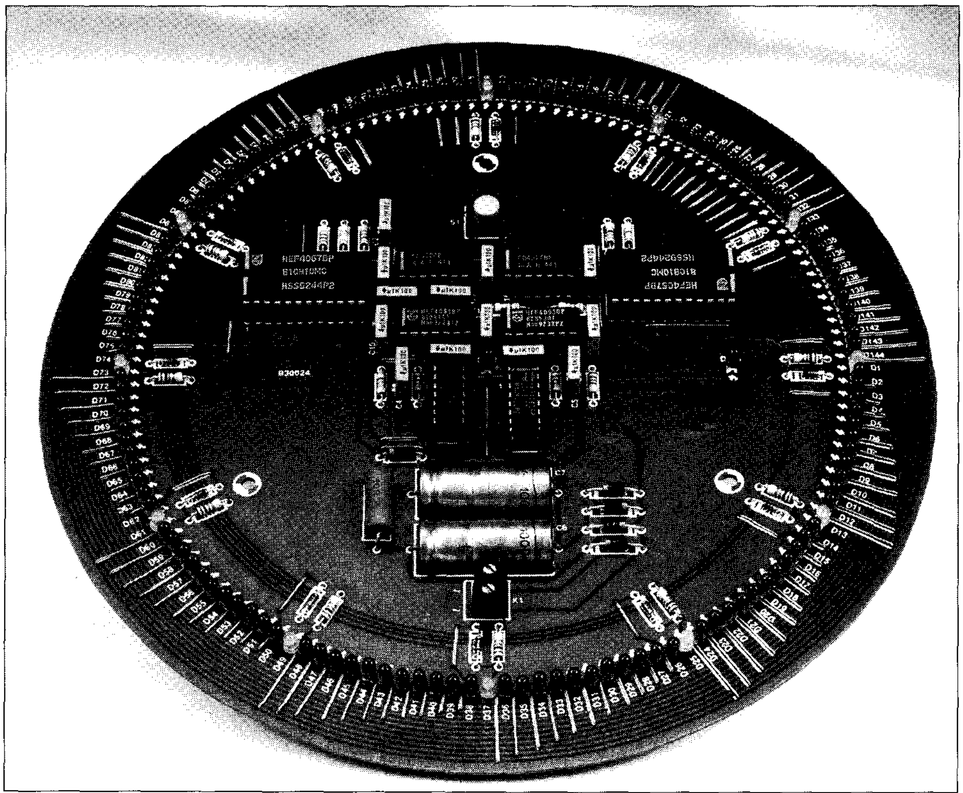
are given in **Fig. 3**. Unfortunately, the position of the LEDs in a circle requires a fair number of wire links on the board.

The board which comes through our Readers Services is square, and may be made round with the aid of a jigsaw before any components are fitted. The circuit board underneath C_6 and C_7 has to be cut out to give these capacitors a recessed mounting.

After the sawing work, start the electronic construction by fitting the wire links. Next, all parts may be mounted. Because the clockwork will have to be as flat as possible, it is necessary to mount the LEDs close to the board surface. Also use miniature ceramic decoupling capacitors. If you are confident about your soldering skills, you may fit the ICs without sockets.

The clock will start to work the moment the 9-V transformer is connected to terminal block K_1.

Assuming that the clockwork is hung up with K_1 down and push-button S_1 up, the first green LED to light will be D_1. The time indicated is then three o'clock. Every time S_1 is pressed, the clock is advanced five minutes.



The finishing touches to the clock depend on your own creativity. For instance, the dial may be covered by a round bezel, which partly obscures the components, but leaves the active LEDs clearly visible. Alternatively, a piece of perspex leaves 'the works' in sight. And that, arguably, will be the best option for the true electronics enthusiast. (930024)

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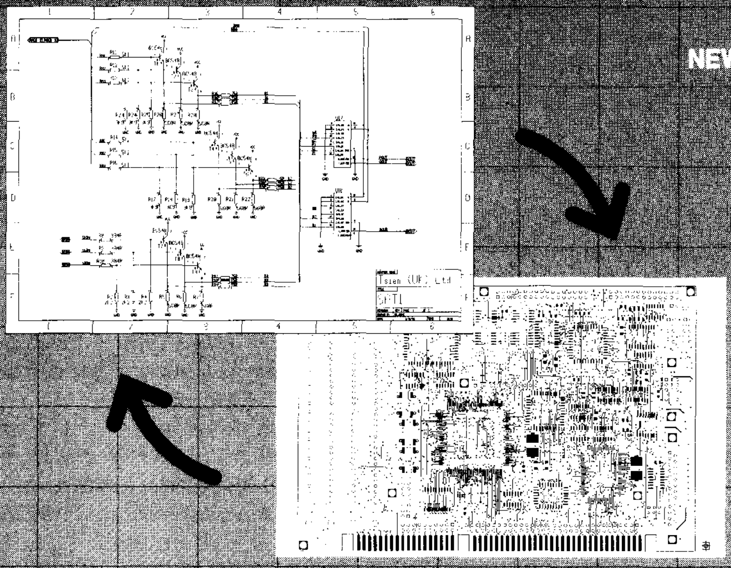

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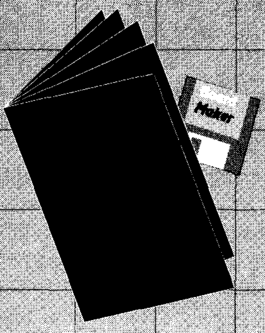

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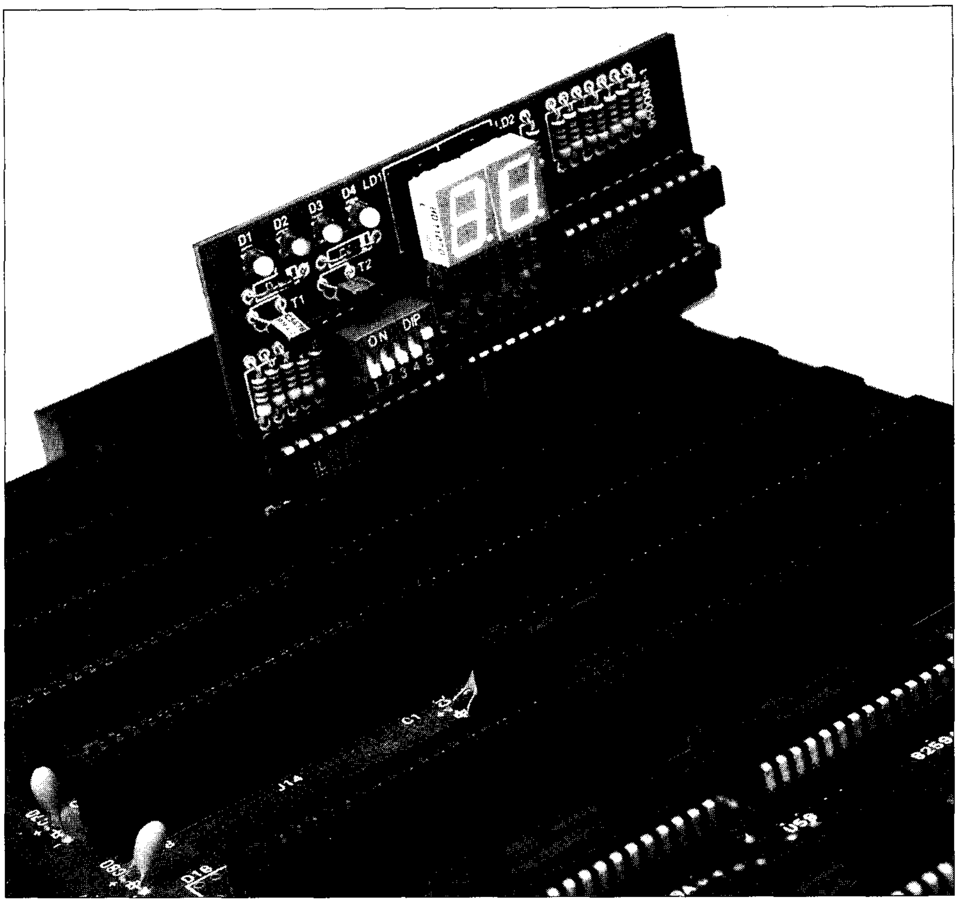
FOCUS ON: DEBUGGING PCs

A P.O.S.T. DIAGNOSTIC CARD

This article, apart from giving some insight into the cause of errors that can occur in a PC, presents a power-on self-test (P.O.S.T.) card which provides a number of powerful hardware fault tracing utilities.



Design by M. Rathjen

USING a PC is one thing, getting it to work again after a major crash is another kettle of fish. What do you do if the machine fails to boot all of a sudden, and only produces a couple of short beeps at power-on? That will typically happen when the guarantee period has just expired, and you are hard pressed to get a report out by the deadline.

As of the IBM PC/AT, an 80286-based PC introduced in 1983, every PC, be it a 386, 486 or Pentium type, has a built-in power-on self test function (P.O.S.T.). In most PCs, the power-up booting sequence is performed in steps, leaving certain codes at port address 80H. The meaning of this 'diagnostic' code may be found in a list which is supplied (rarely, though) by the manufacturer of the BIOS (basic input output system) ROMs in the PC. Although P.O.S.T. codes are not intended for the end user, they do provide useful information on what goes wrong in a faulty PC during the crucial boot-up phase. After all, if the machine does not get past the self-testing phase, you will be unable to load and run special diagnostic programs from disk.

The half-length 8-bit insertion card described here captures and indicates the P.O.S.T. code on a pair of 7-segment displays. It may be configured to read other port addresses as well, and also gives a present/absent indication of the PC's four power supply voltages.

MAIN SPECIFICATIONS

Card address:	user selectable, 60H, 80H, 84H, 90H, 280H or 300H.
PSU check:	4 LEDs
Display:	hexadecimal, 2-digit 7-segment LED
Card type:	8-bit, ISA, through-plated

General points

Immediately after the PC is switched on, some pretty rigorous testing is done on the internal hardware. The BIOS integrates a number of routines which check out nearly everything inside the PC, from the memory to the interrupt (IRQ) routines. Before each test, the BIOS sends the corresponding P.O.S.T. code to the diagnostic port. If the PC remains 'stuck' in a certain test routine, the associated P.O.S.T. code will remain on the display, allowing you to start thinking about a possible cause of the problem.

Let us take an example: an AT/386 machine fitted with an AMI BIOS v. 2.21 crashes at P.O.S.T. code 27H. According to the information in **Table 1** (overleaf) this code means that an error has occurred in the 64-Kbyte base memory test. Quite likely, the fault is in one of the memory chips, or in a SIPP or SIMM module.

The appendices with this article show the P.O.S.T. codes for a number of popular BIOS ROMs. Unfortunately, owing to space restrictions, the information is not exhaustive. If your PC has a BIOS which is not listed, contact the manufacturer to obtain a copy of the P.O.S.T. code set.

The electronics

In view of the simplicity of the P.O.S.T. insertion card, a block diagram is not given. So, let us move on straight away to the circuit diagram, which is presented in **Fig. 1**. A pair of GALs (generic array logic) simplifies the circuit considerably because these ICs contain a fair number of logic circuits. GAL IC_1 functions as the card address

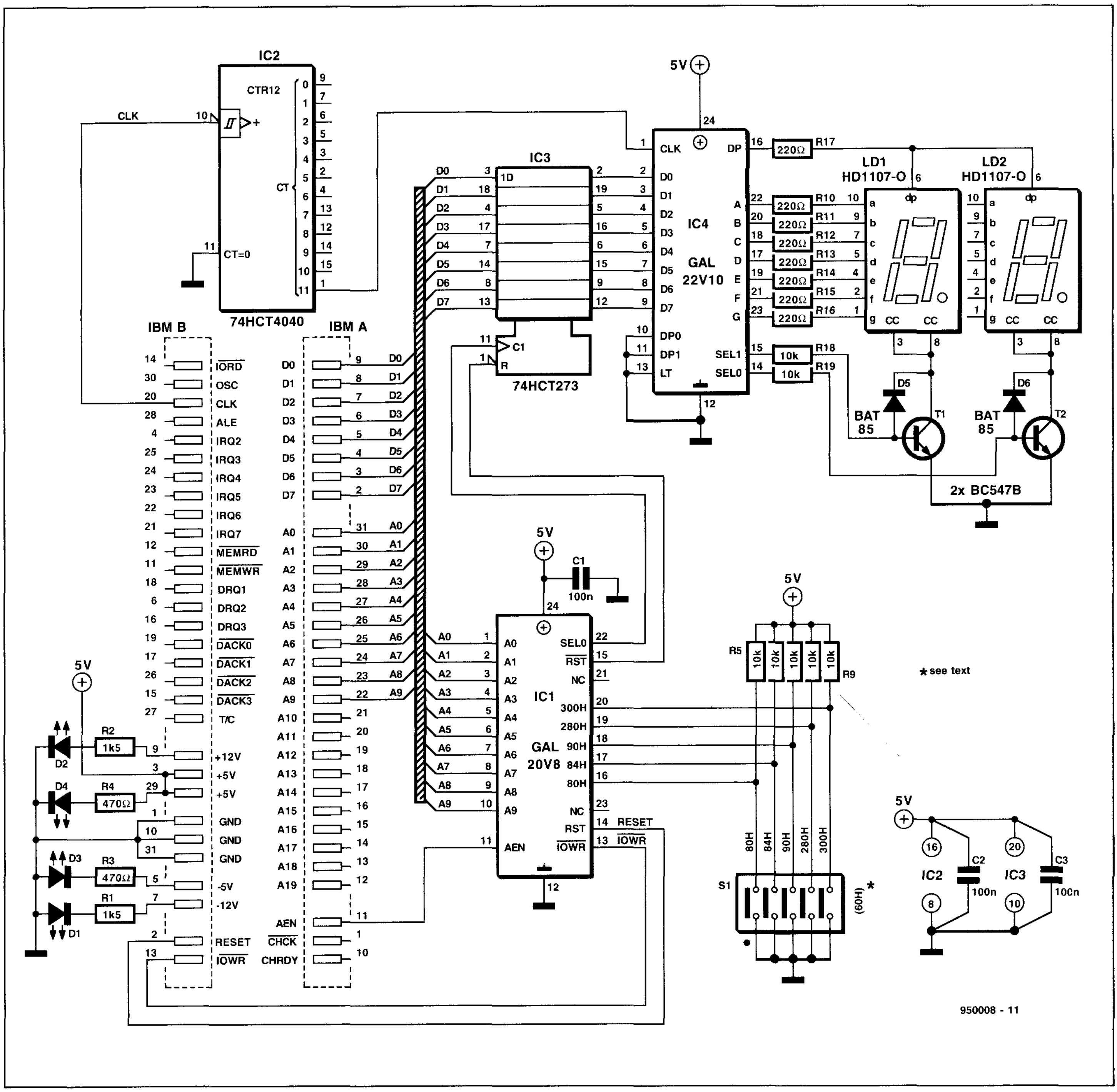


Fig. 1. Circuit diagram of the P.O.S.T. diagnostic card. Simple and effective as a stethoscope! The use of two GALs results in a remarkably low component count.

decoder. It also reads the address set on a 5-way DIP switch. This is necessary because PC manufacturers unfortunately have not agreed on a standard address. The address setting will be reverted to further on. The advantage of a GAL over the ubiquitous '688 address decoder is that it is capable of instantaneous address comparison, i.e., not incremental-binary.

GAL IC_1 performs Boolean logic using address lines A0 and A9, plus control lines AEN (address enable) and IOWR (input/output write) as input variables. It also reads the logic levels supplied by DIL switch S_1. The default port address setting is 60H (yes, for XTs), since that is not listed as one of the possibilities in Fig. 1. Remember, we are dealing with hexadecimal numbers here. For example, address 300H is selected if both A8 and A9 are logic high, and all other address lines, logic low (see **Table 2**).

The second GAL, IC_4, is programmed to function as a dual BCD-to-7 segment decoder (see Ref. 1), turning the output codes supplied by octal bistable IC_3 (74HCT273) directly into drive signals for the LED segments. Current limiting is provided by a resistor network. Apart from reducing the component count, the GAL also extends the possibilities of most conventional BCD-to-7 segment decoders by being able to display hexadecimal numbers also. The 7-segment LED displays are common-cathode types. The current flow is, therefore, from the positive supply line, via the GAL outputs, current limiting resistors (220 Ω) and a transistor c-e junction, to ground.

Circuit IC_2 divides the system clock down to a value suitable for multiplex-

POST Codes - AMI BIOS 2.2X

00 : Flag test
03 : Register test
06 : System hardware initialization
09 : BIOS ROM checksum
0C : Page register test
0F : 8254 timer test
12 : Memory refresh initialization
15 : 8237 DMA controller test
18 : 8237 DMA initialization
1B : 8259 interrupt controller initialization
1E : 8259 interrupt controller test
21 : Memory refresh test
24 : Base 64K address test
27 : Base 64K memory test
2A : 8742 keyboard self test
2D : MC146818 CMOS test
30 : Start first protected mode test
33 : Memory sizing test
36 : First protected mode test
39 : First protected mode test failed
3C : CPU speed calculation
3F : Read 8742 hardware switches
42 : Initialize interrupt vector area
45 : Verify CMOS configuration
48 : Test and initialize video system
4B : Unexpected interrupt test
4E : Start Second protected mode test
51 : Verify LDT instruction
54 : Verify TR instruction
57 : Verify LSL instruction
5A : Verify LAR instruction
5D : Verify VERR instruction
60 : Adress line 20 Test
63 : Unexpected exception test
66 : Start third protected mode test
69 : Address line test
6C : System memory test
6F : Shadow memory test
72 : Extended memory test
75 : Verify memory configuration
78 : Display configuration error messages
7B : Copy system BIOS to shadow memory
7E : 8254 clock test
81 : MC146818 real time clock test
84 : Keyboard test
87 : Determine keyboard type
8A : Stuck key test
8D : Initialize hardware interrupt vector
90 : Math coprocessor test
93 : Determine COM ports available
96 : Determine LPT ports available
99 : Initialize BIOS data area
9C : Fixed/Floppy controller test
9F : Floppy disk test
A2 : Fixed disk test
A5 : External ROM scan
A8 : System key lock test
AE : F1 error message test
AF : System boot initialization
B1 : Interrupt 19 boot loader

Table 1. POST codes for version 2.2 of the BIOS supplied by American Megatrends Inc.

Address line	**A9**	**A8**	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
Decimal	512	256	128	64	32	16	8	4	2	1
Hexadecimal	200	100	80	40	20	10	8	4	2	1

Table 2. Card address selection. Example: using address lines A8 and A9 selects address 300H (100H + 200H = 300H).

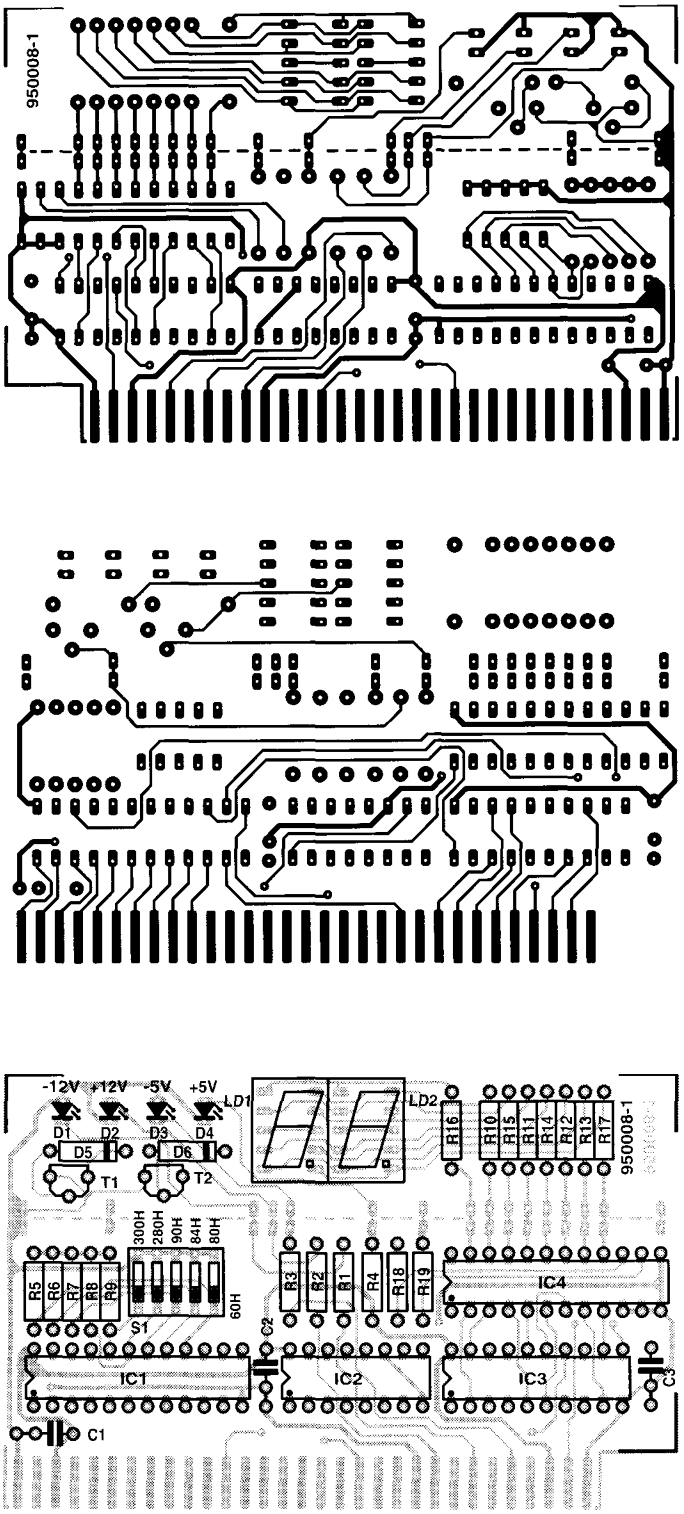


Fig. 2. Track layout (direct reading) and component mounting plan of the P.O.S.T. diagnostic insertion card. The upper part (display) may be cut off and fitted separately at an angle of 45°.

ing the displays. Both GALs used in this circuit are supplied ready-programmed through our Readers Services.

The four LEDs in the circuit indicate the presence of the following supply voltages (LEDs left to right on the board): +5 V, +12 V, −12 V, + 12V. It should be noted that these LEDs merely provide a yes/no indication about the presence of the relevant supply voltage — they do not provide information on the exact levels. If you seek assurance, use your multimeter to establish the exact voltage levels.

As already mentioned, the DIP switch allows you to set the port address required for your specific brand of computer. Consult **Table 3** for the setting you need.

Build a P.O.S.T.card

The card can be built successfully by anyone who works accurately, and uses the printed circuit board supplied through our Readers Services. The artwork of this printed circuit board is given in **Fig. 2**. The board may be cut into two to separate the control section from the display section. Depending on your specific application, you may also leave it intact, however.

As usual, start the construction by fitting the low-profile passive parts, resistors and capacitors. Proceed with

continued on p. 64

COMPONENTS LIST

Resistors:
R_1;R_2 = 1kΩ5
R_3;R_4 = 470Ω
R_5-R_9;R_{18};R_{19} = 10kΩ
R_{10}-R_{17} = 220Ω

Capacitors:
C_1-C_4 = 100nF

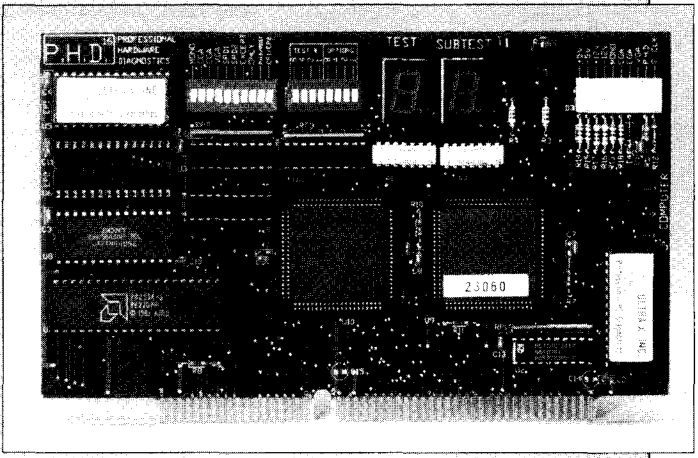
Semiconductors:
D_1-D_4 = LED, red, 3mm dia.
D_5;D_6 = BAT85
T_1;T_2 = BC547B
IC1 = GAL20V8 (order code 946639-1, see page 78)
IC_2 = 74HCT4040
IC_3 = 74HCT273
IC_4 = GAL22V10 (order code 946639-2, see page 78)
LD_1;LD_2 = HD1107O (Siemens)

Miscellaneous:
S_1 = 5-way DIP switch.
Printed circuit board plus 2 programmed GALs, set order code 950008-C (see page 78).

PC DIAGNOSTIC HARDWARE

Market research for 8- and 16-bit PC diagnostic cards shows that there are relatively few products available. On being approached for photographs and descriptions of their products, only one manufacturer of P.O.S.T. diagnostic cards, Industrial Computer Source[1], responded positively. Three of their products are briefly described.

Diagnostic P.O.S.T. Board (model R.A.C.E.R. II*)*
This card enables the cause of faults on any PC motherboard, from 8088 to 80486, to be traced and evaluated. The results of the diagnostic operation are shown on the PC screen, a set of LED displays, or on a printer.



Advanced 16-bit Diagnostic Card (model PHD16)
This is an even more powerful card than the R.A.C.E.R. The PHD16 runs a large number of tests in a wide range of hardware sub-sections, including DMA (direct memory access) and IRQ (interrupt request). Thanks to the intelligent electronics on this card, it uses only a small number of functions of the system under test. Consequently, the board is able to locate faults on motherboards which look absolutely 'dead'.

Micro-Toolkit
This kit, manufactured by 2000 Micro Diagnostics[2], and supplied via Industrial Computer Source, contains a diagnostic program called 'Micro-Scope', a P.O.S.T. diagnostic card, and a P.O.S.T. probe. Armed with these powerful tools you should be able to trace and eliminate any malfunction on a PC motherboard. Extremely effective, the kit even allows low-level formatting of hard disks (including IDE types). It also has its own examination system, and enables all types of memory to be tested, including cache, video, RAM, etc.

The following P.O.S.T. diagnostic cards are also available, unfortunately no product descriptions were received from the relevant manufacturers:
the **V-ATE Plus** from Vista Microsystems, Inc.
the **POST Code Display** from JDE Microdevices.

---

[1] Industrial Computer Source, European Headquarters, Z.A. de Courtaboeuf, 16 Avenue du Quebec, B.P. 712, F-91961 Les Ulis Cedex, France. Tel. (+33) 1 69.07.28.22, Fax (+33) 1 64.46.40.42. UK readers please contact Industrial Computer Source (UK) Ltd., Birdham Road, Chichester, W. Sussex PO20 7EQ, England. Tel. (01243) 533900, fax (01243) 532949.

[2] Micro 2000, Inc. 1100 East Broadway, Suite 301, Glendale, CA 91205, U.S.A. Tel. (+1) 818/547-0125 or (+1) 800 864-8008, fax (+1) 818/547-0397.
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MAINS IONIZER KIT. Very useful kit that increases the flow of negative ions, helps clear cigarette smoke, dust, pollen etc. Helps reduce stress and respiratory problems. £15. kit, £20 built.

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VARIABLE POWER SUPPLY. Stabiized, short circuit protected. Gives 3-30v DC at 2.5A, ideal for workshop or laboratory. £14 kit,£18 built. 24VAC required.

LEAD ACID CHARGER. Two automatic charging rates(fast and slow), visual indication of battery state. Ideal for alarm systems,emergency lighting, battery projects etc. £12 kit,£16 built.

PHONE LINE RECORDER.Device that connects to the 'phone line and activates a cassette recorder when the handset is lifted. Ideal for recording 'phone conversations etc!. £8 kit, £12 built.

ROBOT VOICE. Turns your voice into a robot voice! answer the phone with a different voice!. £9 kit, £13 built.

PHONE BUG DETECTOR. This device will warn you if somebody is eavesdropping on your 'phone line. £6 kit £9 built.

PHONE BUG. Small bug powered by the telephone line. Only transmits when the phone is used. Popular surveillance product.£8 kit, £12 built.

STROBE LIGHT. Bright strobe light with an adjustable frequency of 1-60hz. (a lot faster than conventional strobes!) £16 kit, £20 built.

4W FM TRANSMITTER. 3 RF stages, audio preamp. 12-18vDC. Medium powered bug £20 kit, £28 built.

3 CHANNEL LIGHT CHASER. 3x 800w output, speed and direction controls, can be used with 12 led's (supplied) or TRIACS for mains lights (also supplied). 9-15v DC. £17 kit, £23 built.

25W FM TRANSMITTER. 4 stage, a preamp will be required. (Our preamp below is suitable) £79 built.(no kits).

SOUND EFFECTS GENERATOR. Produces any thing from bird chips to sirens! add sounds to all sorts of things £9 kit £13 built.

FM/AM SCANNER. Well not quite,you have to turn the knob yourself but you will hear things on this radio (even TV) that you would not hear on an ordinary radio! A receiver that covers 50-160MHZ both AM and FM. Built in 5w amplifier. £15 kit, £20 built.

CAR ALARM SYSTEM. Works on vibration and/or voltage drop from door etc being opened. Entry and exit delays plus adjustable alarm duration. Low cost protection! £12 kit, £16 built.

15W FM TRANSMITTER. 4 stage, high power bug. You will need a preamp for this (see our preamp below which is ok) £69 built. (no kits).

1W FM TRANSMITTER. 2 stage including preamp and mic. Good general purpose bug. 8-30VDC. £12 kit,£16 built.

50 I/C's for £1.50
Nice mix of chips at a bargain price!

CERAMIC CAPACITOR PACK
Good mixed pack of 100 capacitors for just £1.00

ELECTROLYTIC PACK 1
100 small mixed electrolytic capacitors just £1.00

ELECTROLYTIC PACK 2
50 larger electrolytic mixed capacitors

RESISTOR PACK NO 1
250 low wattage resistors, ideal for most projects etc. Just £1.00

RESISTOR PACK NO 2
Hi wattage pack, good selection of mixed wattages and values 50 in all, bargain price just £1.00

PRESET PACK
Nice selection of 25 mixed preset pots for just another £1!

RELAY PACK NO 1
6 mixed relays for £1, thats just 17p each.

CONNECTOR PACK
10 different connectors, again for £1

FUSE PACK NO 1
40 mixed 20mm fuses, ideal for repairs etc, or just to stock up the spares box! Just £1.00

FUSE PACK NO 2
30 mixed 1.25" fuses again ideal for spares etc. Just £1.00

WIRE PACK
25 Metres of insulated wire for just £1.00, good for projects etc.

SLEEVING PACK
100 assorted pieces of sleeving for connectors etc. Yours for just £1.00

DIODE PACK
100 assorted diodes for just £1.00

LED PACK
20 light emitting diodes for £1.00

TRANSISTOR PACK
50 mixed transistors, another bargain at £1.00

BUZZER PACK
10 things that make a noise for just £1.00!

POT PACK
10 pots for £1, (5 different types) a snip at £1.00

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10 seven segment displays for £1.00

ORDER 10 PACKS OR MORE AND CHOOSE ONE FREE PACK!!

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99p Post

BULK PACKS

PREAMP MIXER. 3 channel input, independent level and tone controls. Ideal for use with the hi power FM transmitters. £15 kit, £19 built.

TREMBLER ALARM. Designed for bikes etc, adjustable sensitivity, preset alarm time, auto reset. Could be adapted for all sorts of "borrowable" things £12 kit,£16 built.

ULTRASONIC RADAR. A project that can be used as a movement detector in an enclosed space. Range about 10 metres, 12vDC. Good basis for car,shed,caravan alarm etc.£14 kit, £19 built.

PHONE CALL RELAY. Very useful kit that incorporates a relay that operates when the phone rings. Can be used to operate more bells, signalling lights etc. Good for noisy enviroments or if you have your headphones on! £10 kit, £14 built.

PORTABLE ALARM SYSTEM. Small 9v alarm system based on a mercury switch. The alarm contitues to sound until disabled by the owner. Buzzer included. £11 kit £15 built.

800W MUSIC TO LIGHT EFFECT. Add rhythm to your music with this simplesound to light kit. £8 kit, £12 built.

MOSQUITO REPELLER. Modem way to keep the midges away! Runs for about a month on one 1.5v battery. Frequency is set to drive away mosquitos etc. £7 kit, £11 built.

3 CHANNEL SOUND TO LIGHT. Can be used anywhere as no connection is made to hi fi. Separate sensitivity controls for each channel, 1,200W powerhandling. Microphone included. £14 kit, £19 built.

MINI METAL DETECTOR. Detects pipes,wires etc up to 20cm deep. Useful before you drill those holes! £8 kit, £12 built.

0-5 MINUTE TIMER. Simple time switch adjustable from 0-5 mins,will switch 2A mains load. 12v op. Ideal for laboratory, photographic projects etc. £7 kit, £11 built.

7 WATT HI FI AMPLIFIER. Useful, powerful amplifier 20hz-15hz, 12-18vdc. Good for intercoms, audio systems, car etc. £7 kit £11 built.

INCAR SOUND TO LIGHT. Put some atmosphere in your car with this kit. Each channel has 6 led's that create a beautiful lighting effect! £10 kit, £14 built.

VOX SWITCH. This is a sound activated switch, ideal for use on transmitters, CB's, tape recorders etc. Adjustable sensitivity, built in delay. Mic input. £7 kit, £11 built.

KITS 'N MODULES

LIQUID LEVEL DETECTOR. Useful item, can be used to detect fluid levels in watertanks, baths, ponds fishtanks etc. Could also be used as rain alarm with an easily constructed sensor. £5 kit, £9 built.

FM TRANSMITTER. Mini FM transmitter 2 transistor, comes with FET minature mic and is tuneable from 63 to 130MHZ. £7 kit, £11 built.

FUNCTION GENERATOR. Generates sinusoidal, saw tooth and square waveforms from 20hz up to 20khz. Separate level controls for each waveform. 24vac. £15 kit, £20 built.

5 WATT SIREN. Powerful siren kit with an impressive 5 watts output. Ideal for alarms etc. £6 kit £10 built.

TELEPHONE AMPLIFIER. Very sensitive amplifier which using a 'phone pickup coil (supplied) will let you follow a telephone conversation without holding the handset to your ear! £11 kit £15 built.

SWITCH PACK
10 switches for just £1.00

12v FLOURESCENT. A useful kit that will enable you to light large flourescent tubes from your car battery etc. 9v mains transformer required. £8 kit, £12 built.

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10 knobs for just £1.00

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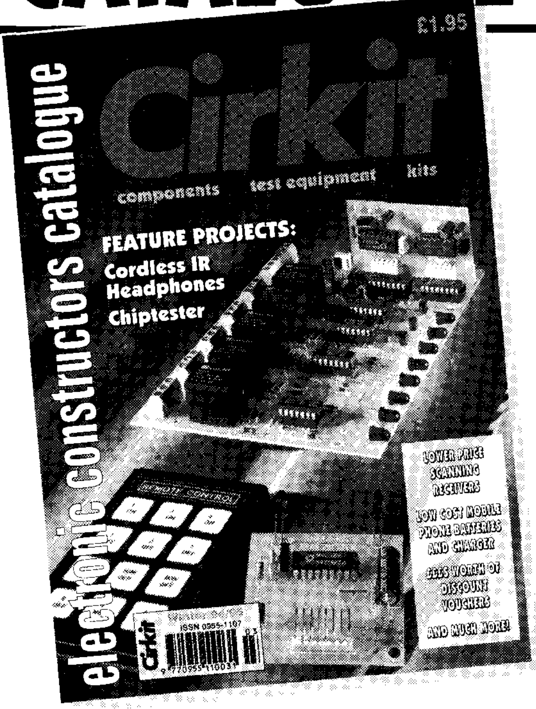
Cheques and postal orders should be payable to Express Components.
ALL PRICES ARE SUBJECT TO 99p POST AND VAT. Some of our products may be unlicensable for use in the UK (particularly the FM transmitters.)

WINTER 1994/5 CATALOGUE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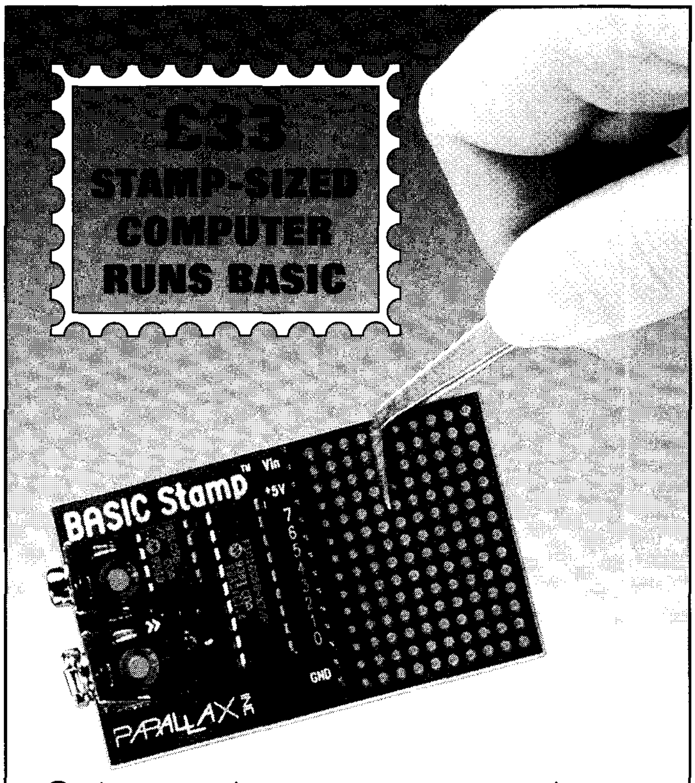

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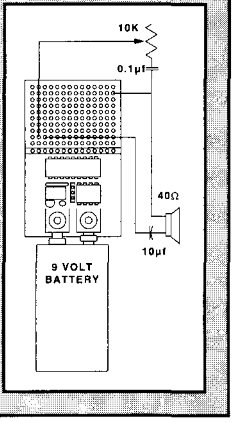

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PC DIAGNOSTIC SOFTWARE

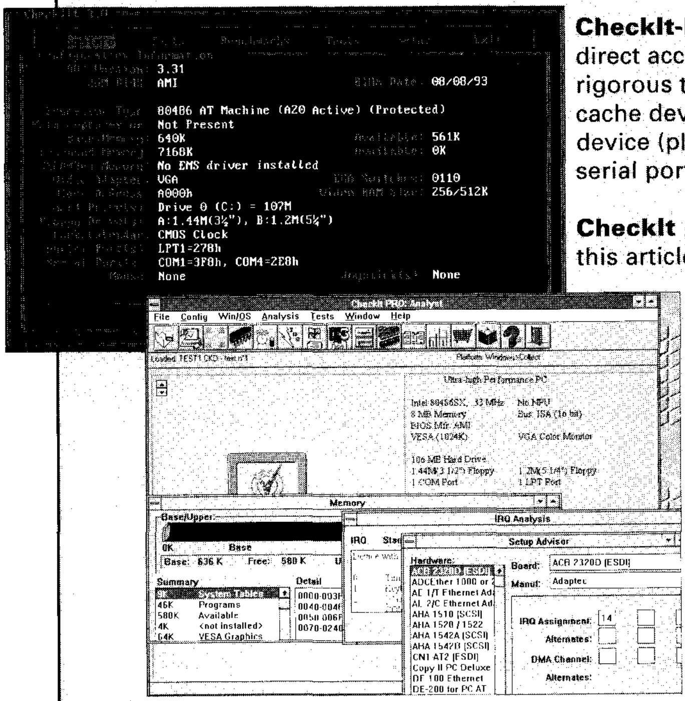
It will be clear that the programs mentioned here are only useful if the essential hardware of the PC is functional. This goes for commercially available programs such as Checkit, Checkit Analyst and QuickTech Pro, as well as those in the shareware domain. So, hardware debugging goes logically before running any of the programs mentioned in this inset.

CheckIt-Pro diagnostic software is typical of its class. The program ensures direct access to the most essential (i.e., critical) functions of the system, using rigorous tests on the CPU, all types of memory, internal as well as external cache devices, video, RAM, etc. It also scrutinizes each and every peripheral device (plug-in cards) connected to the motherboard, including parallel and serial ports, the keyboard, video cards, hard disk, and others.

CheckIt Analyst was also examined as part of the research carried out for this article. The program can be run on DOS, Windows or OS/2 platforms. Great performance if you are after elusive faults in, say, the realms of IRQ, memory or input output addresses.

Troubleshooter also runs extremely intricate tests on all system components, from CPU to peripherals and, of course, the memory (which for some reason seems to be the most troublesome area). It even does a quick test on a CD-ROM player (hard to imagine, though, with, say, a PC/XT clone) and a sound card, if installed.

Surprisingly, there is a program which most of you will have but appears to be little known. **MSD**, MicroSoft Diagnostic, is included in your Windows 3.1 (and later) package, and can be found in the Windows subdirectory. It should be noted, however, that the first aim of MSD is to establish exact system configurations, rather than assisting in locating hardware faults.



```
3.31
AMI                                  08/08/93

80486 AT Machine (A20 Active) (Protected)
Not Present
640K                                 561K
7168K                                0K
No EMS driver installed
VGA                                  0110
A000h                                256/512K
Drive 0 (C:) = 107M
A:1.44M(3½"), B:1.2M(5¼")
CMOS Clock
LPT1=278h
COM1=3F8h, COM4=2E8h
None                                 None
```

CheckIt PRO: Analyst
File Config Win/OS Analysis Tests Window Help
Loaded: TEST1.CKD - test n°1
Platform: Windows Collect
Memory
IRQ Analysis
Setup Advisor

Ultra-high Performance PC

Intel 80486SX, 33 MHz — No NPU
8 MB Memory — Bus: ISA (16 bit)
BIOS Mfr: AMI
VESA (1024K) — VGA Color Monitor

106 MB Hard Drive
1.44M(3 1/2") Floppy — 1.2M(5 1/4") Floppy
1 COM Port — 1 LPT Port

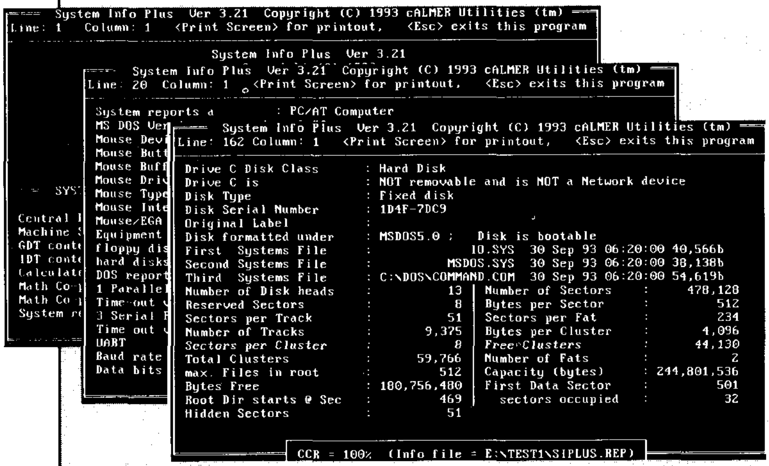
Base/Upper:
0K Base
Base: 636 K Free: 580 K

Summary	
9K	System Tables
46K	Programs
580K	Available
4K	<not installed>
64K	VESA Graphics

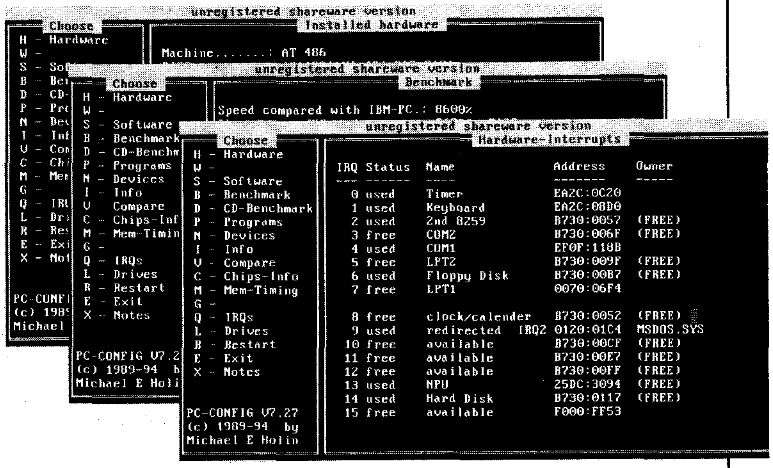
Detail: 0000-003F, 0040-004F, 0050-006F, 0070-0240

Hardware:
ACB 2320D (ESDI)
ADCEther 1000 or 2
AE 1/T Ethernet Ad
AE 2/C Ethernet Ad
AHA 1510 (SCSI)
AHA 1520 / 1522
AHA 1542A (SCSI)
AHA 1542B (SCSI)
CNT AT2 (FSDI)
Copy II PC Deluxe
DE 100 Ethernet
DE-200 for PC AT

Board: ACB 2320D (ESDI)
Manuf: Adaptec
IRQ Assignment: 14
Alternates:
DMA Channel:
Alternates:

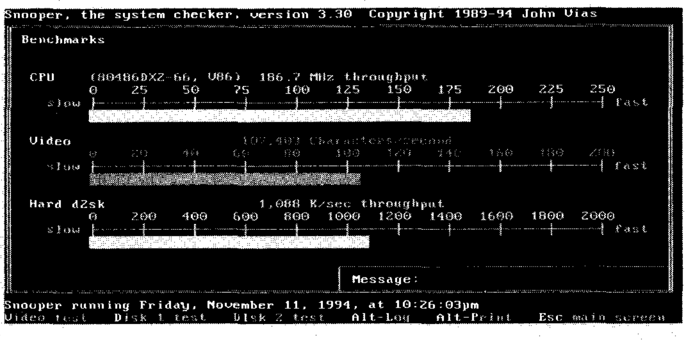


```
System Info Plus  Ver 3.21  Copyright (C) 1993 cALMER Utilities (tm)
Line: 1   Column: 1   <Print Screen> for printout,   <Esc> exits this program

                    System Info Plus  Ver 3.21

System Info Plus  Ver 3.21  Copyright (C) 1993 cALMER Utilities (tm)
Line: 20  Column: 1   <Print Screen> for printout,   <Esc> exits this program

System reports a         : PC/AT Computer

System Info Plus  Ver 3.21  Copyright (C) 1993 cALMER Utilities (tm)
Line: 162 Column: 1   <Print Screen> for printout,   <Esc> exits this program

Drive C Disk Class        : Hard Disk
Drive C is                : NOT removable and is NOT a Network device
Disk Type                 : Fixed disk
Disk Serial Number        : 1D4F-7DC9
Original Label            :
Disk formatted under      : MSDOS5.0 ;   Disk is bootable
First  Systems File       :           IO.SYS  30 Sep 93 06:20:00 40,566b
Second Systems File       :       MSDOS.SYS  30 Sep 93 06:20:00 38,138b
Third  Systems File       : C:\DOS\COMMAND.COM  30 Sep 93 06:20:00 54,619b
Number of Disk heads      :          13 | Number of Sectors     :     478,128
Reserved Sectors          :           8 | Bytes per Sector      :         512
Sectors per Track         :          51 | Sectors per Fat       :         234
Number of Tracks          :       9,375 | Bytes per Cluster     :       4,096
Sectors per Cluster       :           8 | Free Clusters         :      44,130
Total Clusters            :      59,766 | Number of Fats        :           2
max. Files in root        :         512 | Capacity (bytes)      : 244,801,536
Bytes Free                : 180,756,480 | First Data Sector     :         501
Root Dir starts @ Sec     :         469 |   sectors occupied    :          32
Hidden Sectors            :          51

           CCR = 100%  (Info file = E:\TESTI\SIPLUS.REP)
```

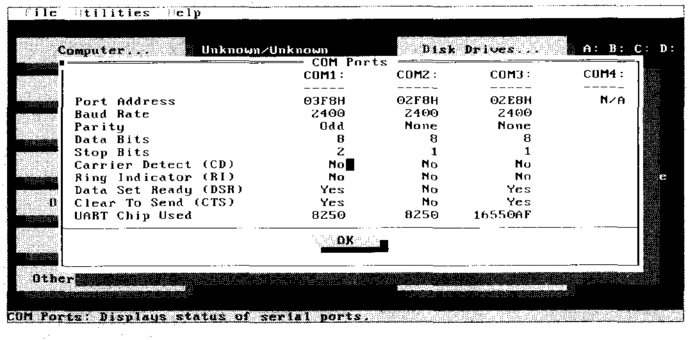


```
unregistered shareware version
Installed hardware
Machine.......: AT 486

unregistered shareware version
Benchmark
Speed compared with IBM-PC.: 8600%

                 unregistered shareware version
Choose                     Hardware-Interrupts
H - Hardware       IRQ Status  Name               Address    Owner
W -                --- ------  ----               -------    -----
S - Software         0 used    Timer              EA2C:0C20
B - Benchmark        1 used    Keyboard           EA2C:08D0
D - CD-Benchmark     2 used    2nd 8259           B730:0057  (FREE)
P - Programs         3 free    COM2               B730:006F  (FREE)
N - Devices          4 used    COM1               EF0F:118B
I - Info             5 free    LPT2               B730:009F  (FREE)
V - Compare          6 used    Floppy Disk        B730:00B7  (FREE)
C - Chips-Info       7 free    LPT1               0070:06F4
M - Mem-Timing
G -                  8 free    clock/calender     B730:0052  (FREE)
Q - IRQs             9 used    redirected   IRQ2  0120:01C4  MSDOS.SYS
L - Drives          10 free    available          B730:00CF  (FREE)
R - Restart         11 free    available          B730:00E7  (FREE)
E - Exit            12 free    available          B730:00FF  (FREE)
X - Notes           13 used    NPU                25DC:3094  (FREE)
                    14 used    Hard Disk          B730:0117  (FREE)
PC-CONFIG V7.27     15 free    available          F000:FF53
(c) 1989-94  by
Michael E Holin
```

Among the best known diagnostic programs in the shareware domain are **S.I. Plus v3.21** (SIPLU321.ZIP) and **Configuration v7.27e** (CONF727E.ZIP), which can found on numerous bulletin boards. The reports created by these programs are very useful if you need to locate and eliminate possible problem sources.



```
Snooper, the system checker, version 3.30  Copyright 1989-94 John Vias
 Benchmarks

 CPU     (80486DX2-66, V86)  186.7 MHz throughput
          0    25    50    75    100   125   150   175   200   225   250
    slow  |-----+-----+-----+-----+-----+-----+-----+-----+-----+-----| fast

 Video                  107,403 Characters/second
          0    20    40    60    80    100   120   140   160   180   200
    slow  |-----+-----+-----+-----+-----+-----+-----+-----+-----+-----| fast

 Hard dZsk               1,088 K/sec throughput
          0    200   400   600   800   1000  1200  1400  1600  1800  2000
    slow  |-----+-----+-----+-----+-----+-----+-----+-----+-----+-----| fast

                                        Message:
Snooper running Friday, November 11, 1994, at 10:26:03pm
Video test   Disk 1 test   Disk 2 test   Alt-Log   Alt-Print   Esc main screen
```



```
File  Utilities  Help

  Computer...      Unknown/Unknown           Disk Drives...     A: B: C: D:
                              COM Ports
                               COM1:      COM2:      COM3:      COM4:
                               -----      -----      -----      -----
   Port Address                03F8H      02F8H      02E8H        N/A
   Baud Rate                    2400       2400       2400
   Parity                        Odd       None       None
   Data Bits                       8          8          8
   Stop Bits                       2          1          1
   Carrier Detect (CD)            No         No         No
   Ring Indicator (RI)            No         No         No
   Data Set Ready (DSR)          Yes         No        Yes
   Clear To Send (CTS)           Yes         No        Yes
   UART Chip Used               8250       8250   16550AF

                               OK
  Other
COM Ports: Displays status of serial ports.
```

Finally, the familiar **Norton Utilities** and **PCTools** packages are not discussed in detail here because their system diagnosis utilities form only a small part of a much wider range of sub-programs and menus. After all, most of the functions offered by these programs come under the header of disk organization and efficient file management.

inserting the ICs into their sockets, taking care to observe the proper orientation. Also be sure to fit the right GAL into the right socket — these devices do not have the same function! The board is not fitted with the usual support bracket at the rear side because it is not intended to remain permanently inside the PC.

Address	PC type/brand	DIP switch S1
60H	XT (default value)	none closed
80H	AT/386/486/Pentium	S$_{1e}$ closed
84H	Compaq	S$_{1d}$ closed
90H	PS/2–30 with ISA bus	S$_{1c}$ closed
280H	Clones (including some Compaq PCs)	S$_{1b}$ closed
300H	EISA bus systems	S$_{1a}$ closed

Table 3. Overview of P.O.S.T. card addresses used in different computer types and brands.

Testing the test card

The completed card is first inserted into one of the free slots of a functional PC. Next, run the Pascal program listed in **Fig. 4**. It is recommended to use the card at base address 300H, which, according to the IBM PC specification, is reserved for experimenting. This address is selected by closing **only** S$_{1a}$ on the DIP switch block. The card is functional if the compiled program produces an incrementing number on the LED display and the PC screen every time you press CR. Note, however, that the LED display readout is hexadecimal, while the numbers on the PC screen are in decimal.

If the P.O.S.T. card does not pass this test, you have probably made a construction error. Start by verifying the presence of a clock signal at pin 11 of latch IC$_3$. If this signal is present, check the latch outputs, which should supply copies of the latch input signals. If this test also checks out, the only likely cause of the malfunction that remains is either GAL IC4 or one of the 7-segment LED displays.

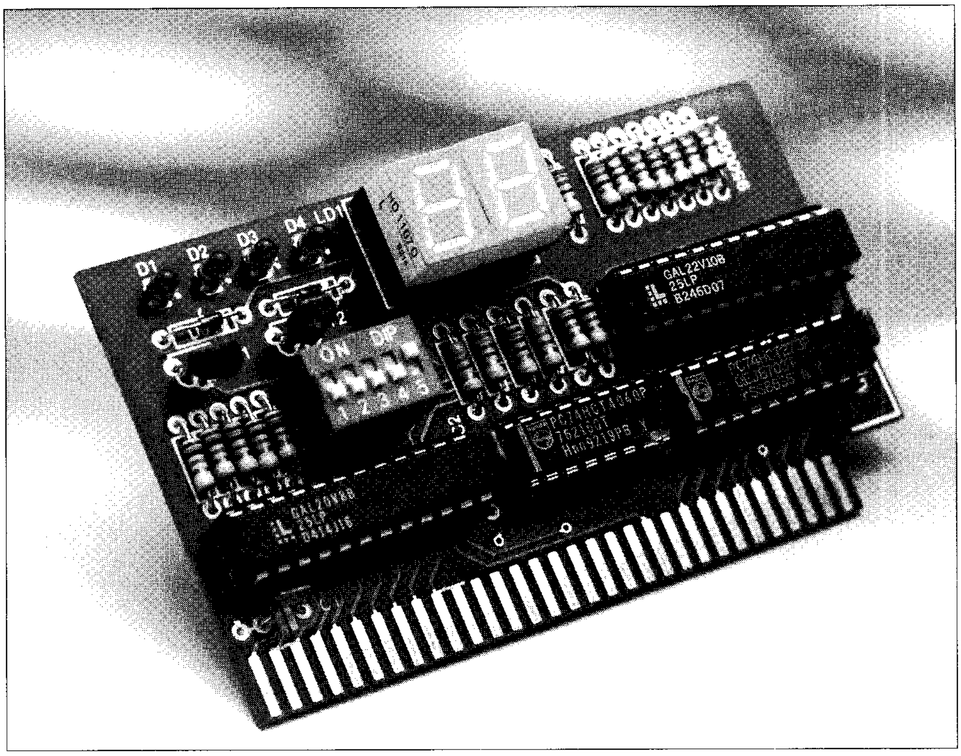


Fig. 3. Completed prototype of the P.O.S.T. diagnostic card. Note that this version differs slightly from the final design.

In case of trouble...

The P.O.S.T. code display card described here does not pretend to be a replacement of much more powerful PC diagnostic cards available commercially. Rather, its function is that of an auxiliary tool. None the less, the present card is extremely valuable if you wish to bring back life to, say, an old 286 motherboard which does not even produce error beeps on being powered. As already mentioned, the aim is to get past the initial test routines (*P.O.S.T. mortem!*), and make sure that the relevant motherboard can load at least the DOS again. From there on, you are in a position to run hardware/software diagnostic tools such as Norton, CheckIt and PCTools.

The P.O.S.T. code displayed by the card supplies a possible cause of the problems experienced with either a component on the motherboard, a memory module, or one of the insertion cards. If the fault appears to be in an extension card, it is relatively simple to resolve by a visit to your local computer shop and replace the culprit. On the other hand, if the problem is at level of, say, the DMA or interrupt controller, or any other complex ASIC or GAL on the motherboard, replacement or repair is probably not worth the effort, and the motherboard is best chucked into the bin after removing the RAM and CPU parts. Incidentally, replacement motherboards with empty CPU sockets may be obtained at very low prices these days. Regrettably, though, it seems almost impossible to obtain spares of the ICs that form the so-called chip set (Neat, etc.) on the motherboard, while desoldering and re-fitting these 'jumbos' is really out of the question without very special tools.

(950008)

Reference:

1. Hexadecimal display decoder, *Elektor Electronics* December 1993.

```
program testpostcard;
uses dos, crt;
   const post = $300;
var
   i : word;
   dummy : char;
begin
   for i:=0 to $ff do
   begin
     port[post]:=i;
     writeln (i);
     repeat until keypressed;
     dummy:=readkey;
   end;
end.
```

Fig. 4. Listing of the test program for the P.O.S.T. diagnostic card (Pascal). Change the value of constant 'Post' as required for your specific brand and type of PC.

Appendix: PC BIOS P.O.S.T codes

all trademarks acknowledged. E. & O.E.

POST Codes - AMI BIOS POST

01 : NMI disabled & 286 reg. test about to start
02 : 286 register test over
03 : ROM checksum ok
04 : 8259 initialization ok
05 : CMOS pending interrupt disabled
06 : Video disabled & system timer counting ok
07 : CH-0 of 8253 test ok
08 : CH-2 of delta count test ok
09 : CH-1 of delta count test ok
0A : CH-0 of delta count test ok
0B : Parity status cleared
0C : Refresh & system timer ok
0D : Refresh link toggling ok
0E : Refresh period ON/OFF 50% ok
10 : Confirmed refresh ON & about to start 64K memory error
11 : Adress line test OK
12 : 64K base memory test ok
13 : Interrupt vector initialized
14 : 8042 keyboard controller test ok
15 : CMOS read/write test ok
16 : CMOS checksum/batery check ok
17 : Monochrome mode set ok
18 : Color mode set ok
19 : About to look for optional video ROM
1A : Optional video ROM control ok
1B : Display memory R/W test ok
1C : Display memory R/W test for alternative display ok
1D : Video retrace check ok
1E : Global equipment byte set for video ok
1F : Mode set call for mono/color ok
20 : Video test ok
21 : Video display ok
22 : Power on message display ok

NOTE : The «ok» appearing after many of these POST codes means that particular code line has executed successfully. It does not necessarily mean that the component to which the code refers has passed or failed.

30 : Virtual mode memory test about to begin
31 : Virtual mode memory test started
32 : Processor in virtuel mode
33 : Memory address line test in progress
34 : Memory address line test in progress
35 : Memory below 1MB calculated
36 : Memory size computation ok
37 : Memory test in progress
38 : Memory initialization over below 1MB
39 : Memory initialization over above 1MB
3A : Display memory size
3B : About to start below 1MB
3C : Memory test below 1MB ok
3D : Memory test above 1MB ok
3E : About to go to real mode (shutdown)
3F : Shutdown successful and entered into real mode
40 : About to disable gate A-20 address line
41 : Gate A-20 line disable successfully
42 : About to start DMA controler test
4E : Address line test ok
4F : Processor in real mode after shutdown
50 : DMA page register test ok
51 : DMA unit-1 base register test about to start
52 : DMA unit-1 channel ok, about to begin CH-2
53 : DMA CH-2 base register test ok
54 : About to test f/f latch for unit-1
55 : f/f latch test both units ok
56 : DMA units 1 & 2 programmed ok
57 : 8259 initialization over
58 : 8259 mask register check ok
59 : Master 8259 mask register ok, about to start slave
5A : About to check timer and keyboard interrupt level
5B : Timer interrupt ok
5C : About to test keyboard interrupt
5D : ERROR! timer/keyboard interrupt not in proper level
5E : 8259 interrupt controller error
5F : 8259 interrupt controller test ok
70 : Start of keyboard test
71 : Keyboard BAT test ok
72 : Keyboard test ok
73 : Keyboard global data initialization ok
74 : Floppy setup about to start
75 : Floppy setup ok
76 : Hard disk setup about to start
77 : Hard disk setup ok
79 : About to initialize timer data area
7A : Verify CMOS battery power
7B : CMOS battery verification done
7D : About to analyze diagnostics test result for memory
7E : CMOS memory size update ok
7F : About to check optional ROM C000.0
80 : Keyboard sensed to enable SETUP
81 : Optional ROM control ok
82 : Printer global data initialization ok
83 : RS232 global data initialization ok
84 : 80287 check/test ok
85 : About to display soft error message
86 : About to give control to system ROM E000.0
87 : System ROM E000.0 check over
00 : Control given to interrupt 19, boot loader

POST Codes - AWARD BIOS 3.3

01 : Keyboard controller (8042)
02 : « «
03 : « «
04 : « «
05 : « «
06 : On-board LSI 07 CPU
08 : CMOS 8254, 8237, 8257 & EPROM
09 : « «
0A : « «
0B : « «
0C : « «
0D : « «
0E : « «
0F : Extended CMOS
10 : Refresh
11 : « «
12 : « «
13 : « «
14 : « «
15 : First 64K RAM
16 : Interrup vector tables
17 : Video initialization
18 : Video memory
19 : interrupt line mask
1A : « «
1B : Battery good
1C : CMOS checksum
1D : CMOS chip
1E : Memory size
1F : Memory verifier
20 : CPU support chips
21 : « «
22 : « «
23 : « «
24 : Protected memory size
25 : Protected memory test
26 : Protected mode
27 : Shadow RAM, cache controller
28 : « «
29 : Reserved
2A : Initialize keyboard
2B : Floppy drive initialization
2C : Serial port initialization
2D : Parallel port initialization
2E : Hard disk initialization
2F : Math coprocessor
30 : Reserved
31 : Optional ROMs
FF : Boot

POST Codes - CHIPS and TECHNOLOGIES

00 : Error in POS registers
01 : Flag register failed
02 : CPU register failed
03 : System ROM failed checksum
04 : DMA controler failed
05 : System timer failed
06 : Base 64K failed address test
07 : Base 64K failed ram test
08 : Interrupt controller failed
09 : Hot interrupt occurred
0A : Timer failed to generate interrupt
0B : CPU still in protected mode
0C : DMA page registers failed
0D : refresh not occurring
0E : Keyboard controller not responding
0F : Could not enter protected mode
10 : GDT or IDT failed
11 : LDT register failed
12 : Task register failed
13 : LSL instruction failed
14 : LAR instruction failed
15 : VERR/VERW failed
16 : Keyboard controller A20 failed
17 : Exception failed / unexpected
18 : Shutdown during memory test
19 : Last used error code
1A : Copyright checksum error
1B : Shutdown during memory sizing
1C : CHIPSet initialization
50 : Initialize hardware
51 : Initialize timer
52 : DMA init
53 : 8259 init

54 : Initialize CHIPSet
55 : Set up BMS configuration
56 : Entering protected mode for first time
57 : Size memory chips
58 : Configure memory chip interleave
59 : Exiting protected mode for first time
5A : Determine system board memory size
5B : Relocate shadow RAM
5C : Configure EMS
5D : Set up wait state configuration
5E : Re-test base 64K RAM after RAM sizing
5F : Test shadow RAM
60 : CMOS test
61 : Video test
63 : Protected mode interrupt test
64 : Test line A20
65 : Test Memory addredd lines
66 : Memory test
67 : Extended memory test
68 : Timer interrupt test
69 : Real-time clock (RTC) test
6A : Keyboard test
6B : Coprocessor test
6C : Seriel port test
6D : Parallel port test
6E : Dual card test
6F : Floppy drive controller test
70 : Fixed disk test
71 : Keylock test
72 : Pointing device test
90 : RAM setup
91 : Calculate CPU speed
92 : Check configuration
93 : BIOS initialization
94 : POD bootstrap
95 : Reset ICs
96 : POS select
97 : VGA power on diagnostic and setup
98 : Adapter POS
A0 : Exception 0 during POD
A1 : Exception 1 during POD
A2 : Exception 2 during POD
C0 : System board memory failure
C1 : I/O channel check activated
C2 : Watchdog time out
C3 : Bus time out

POST Codes - COMPAQ (i/o at 280h, NOT at 80h!)

00 : Initialize flags, MSW, IDTLIN
01 : Read manufacturing jumper
02 : 8042 received read command
03 : No reponse from 8042
04 : Look for manufacturing ROM at E0000
05 : Look for manufacturing ROM at C8000
06 : No manufacturing ROMs
07 : Read CMOS reset code
08 : intialize 8259, 80287
09 : Jump indirect indexed by reset code
0A : Vector via 40:67 reset function
0B : Vector via 40:67 with E01 function
0C : Boot reset function
0D : Test #2 8254 counter 0
0E : Test #2 8254 counter 2
0F : Warm boot

Overall Power Up Sequence Codes
10 : PPI disabled, program times 0 & 1
11 : Initialize (blast) VDU controllers
12 : Clear screen, turn on video
13 : Test timer 0
14 : Disable RTC interrupts
15 : Check battery power
16 : Battery has lost power
17 : Clear CMOS DIAGS
18 : Test base memory first 128K)
19 : Clear and initialize base memory
1A : Initialize and test VDU adapters
1B : Test the system ROM
1C : Test CMOS
1D : Test DMA controller and page registers
1E : Text keyboard controller
1F : Test 286 protected mode
20 : Test real and extended memory
21 : initialize time-of-day
22 : Initialize 287 coprocessor
23 : Test the keyboard and interface
24 : Reset A20 and set default CPU speed
25 : test diskette subsystem
26 : Test fixed disk subsystem
27 : Initialize parallel printer
28 : Perform search for optional ROMs
29 : Test for valid system configuration
2A : Clear screen
2B : Check for invalid time and date
2C : Optional ROM search
2D : Test timer 2
2F : Write to DIAG byte

Base RAM Initialization Codes
30 : Clear first 128K bytes of RAM
31 : Load interrupt vectors 70-77
32 : Load interrupt vector 00-1F
33 : Initialize MEMSIZE and RESETWD
34 : Verify CMOS checksum
35 : CMOS checksum is not valid
36 : Check battery power
37 : Check for game adapters
38 : Check for serial ports
39 : Check for parallel printer ports
3A : Initialize prt and comm timeouts
3B : Flush keyboard buffer

Base RAM Test Codes
40 : Save RESETWD value
41 : Check RAM refresh
42 : Start write cycle of 128K RAM test
43 : Reset parity checks
44 : Start verify cycle 128K RAM test
45 : Check for parity errors
46 : No RAM errors
47 : RAM error detected

VDU Initialization and Test Codes
50 : Check for dual frequency in CMOS
51 : Check CMOS VDU configuration
52 : Start VDU ROM search
53 : Vector to VDU option ROMs
54 : Initialize primary display adaptor
55 : Initialize secondary display adaptor
56 : No display adaptlers installed
57 : Initialize primary VDU mode
58 : Start of VDU test (for each adaptor)
59 : Check existence of adaptor
5A : Blank display, check VDU registers
5B : Start screen memory test
5C : End of test for adaptor, clear memory
5D : Error detected on an adaptor
5E : Test the next adaptor
5F : All adapters successfully tested

Memory Test Codes
60 : Start memory test
61 : Enter protected mode
62 : Start memory sizing
63 : Get CMOS size
64 : Start test of real memory
65 : Start test of extended memory
66 : Save size of real and extended memory
67 : Uptade 128K option installed CMOS bit
68 : Prepare to return to real mode
69 : Back in real mode - test successful
6A : Back in real mode - error during test
6B : Display error messages
6C : End of memory test
6D : Initialize KB OK string
6E : Determine size to test
6F : Start of MEMTEST
70 : Display 000CX KB OK
71 : Test each RAM segment
72 : High order address test
73 : Exit MEMTEST
74 : Parity error on bus after memory test, system halted

80286 Protected Mode Codes
75 : Start of protected mode test
76 : Prepare to enter protected mode
77 : Test software exceptions
78 : Prepare to return to real mode
79 : Back in real mode - no error
7A : Back in real mode - error detected
7B : Exit protected test
7C : High order address test failure
7D : Entered cache controller test
7E : Programming memory cacheability
7F : Copy system ROM to high RAM

8042 And Keyboard Codes
80 : Start of 8042 test
81 : Do 8042 self-test
82 : Check result received
83 : Error result
84 : OK 8042, Init mode = 5D
86 : Start keyboard test, reset keyboard
87 : Got acknowledge, read result
88 : Got result, check it
89 : Test for stuck key
8A : Key seems to be stuck
8B : Test keyboard interface
8C : Got result, check it
8D : End of test, no errors

System Board Test Codes
90 : Start of CMOS test
91 : CMOS seems to be ok
92 : Error on CMOS read/write test
93 : Start of DMA Controller test
94 : Page registers seem to be ok
95 : DMA controller is ok
96 : 8237 Initialization is complete

NCA RAM Test Codes
9A : Start of NCA RAM test
Diskette Test Codes
A0 : Start of diskette tests
A1 : FDC reset active (3F2h bit 2)
A2 : FDC reset inactive (3F2h bit 2)

continued on p. 70

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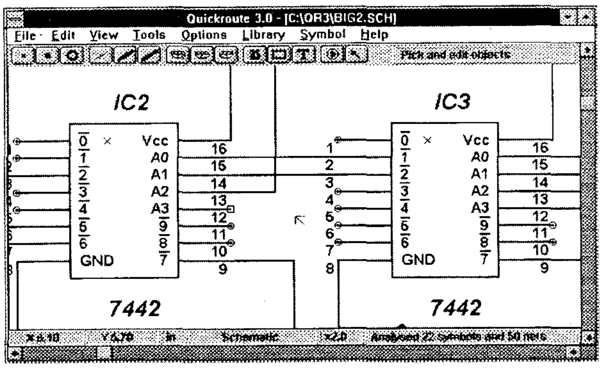
Quickroute 3.0 - [C:\QR3\BIG2.SCH]
File Edit View Tools Options Library Symbol Help
Pick and edit objects
IC2
IC3
Vcc
A0
A1
A2
A3
GND
7442
7442
Schematic

After schematic capture, components can be re-arranged prior to manual or automatic routing.

	Auto Router Max Layers	Schematic Capture	Gerber & NC-Drill	Design Size K nodes
DESIGNER	2 Standard	None	None	10
DESIGNER+	2 Medium	None	Export	20
PRO	8 Fast	Standard	Export	30
PRO+	8 Fast	Advanced	Export/ Import*	40

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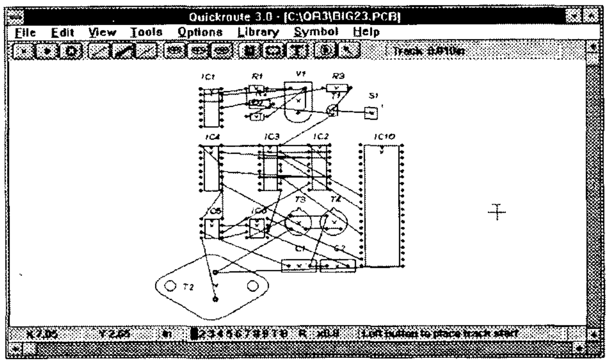
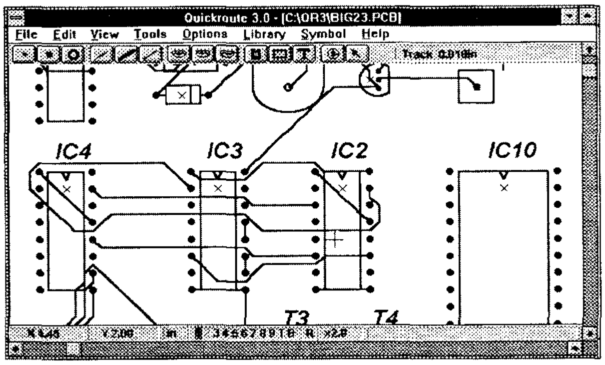

Quickroute 3.0 - [C:\QR3\BIG23.PCB]
File Edit View Tools Options Library Symbol Help
Track 0.010in
IC1
R1
IC4
IC3
IC2
IC10
T2
Left button to place track start


Quickroute 3.0 - [C:\QR3\BIG23.PCB]
File Edit View Tools Options Library Symbol Help
Track 0.010in
IC4
IC3
IC2
IC10
T3
T4

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A3 : FDC motor on
A4 : FDC time-out error
A5 : FDC failed reset
A6 : FDC passed reset
A8 : Start to determine drive type
A9 : Seek operation initiated
AF : Diskette tests complete
B0 : Start of fixed drive tests
B1 : Combo board not found, exit
B2 : Combo controller failed, exit
B3 : Testing drive 1
B4 : Testing drive 2
B5 : Drive error (error condition)
B6 : Drive failed (failed to respond)
B7 : CMOS RAM invalid or no fixed drives, exit
B8 : Fixed drive tets complete
B9 : Attempt to boot diskette
BA : Attempt to boot fixed drive
BB : Boot attempt failed (diskette or fixed)
BC : Boot record read, jump to boot record
BD : Drive error, retry booting
BE : Weitek coprocessor test
D0 : Entry to clear memory routine
D1 : ready to go to protected mode
D2 : Ready to clear extended memory
D3 : Ready to reset back to real mode
D4 : Back in real mode
D5 : Clear base memory
DD : Built-in self-test failed

Option ROM Replacement
E0 : Ready to replace E000 ROM
E1 : Completed E000 ROM replacement
E2 : Ready to replace EGA ROM
E3 : Completed EGA ROM replacement

POST Codes - IBM AT

01 : 80286 processor test (real mode)-flags, regs & cond jmps
02 : ROM checksum test - test 32K ROM POST, BASIC & BIOS
03 : CMOS shutdown byte test - rolling bit ptrn Q shutdown addr
04 : 8254 timer 1 all bits ON - set timer count, check all bits ON
05 : 8254 timer 1 all bits OFF - set timer count, check all bits OFF
06 : 8237 DMA 0 int. chan. reg. test disable DMA cont=0, r/w cur. addr. all ch.
07 : 8237 DMA 1 int. chan. reg. test disable DMA cont=1, r/w cur. addr. all ch.
08 : DMA page register test - read/write all page registers
09 : Storage refresh test - verify refresh is occurring
* 8042 interface test 10 issue self test - check 55H is received
0A : Soft reset
0B : Reset 8042
0C : Test ok
0D : Write byte 0 of 8042 memory
* base 64K r/w memory test - r/w date patters AA, 55, FF, 01 and 00 to first
64K of memory and verify storage addressability
0E fill memory with data
0F : Get I/P buffer switch setting
10 : Roll error code to MFG PORT
11 : Initialize display row count
* Verify 286 LGDT/SGDT LIDT/SIDT instruction
12 : Test protected mode registers
13 : Initialize 8259 int. # controller chip
14 : Setup int. vector to temp. interrupt
15 : Establish BIOS int. call subr. vectors
* Verify CMOS checksum/Battery ok (config ok for init?)
16 : Set data segment
17 : Set defective baterry flag
18 : Ensure CMOS dividers set
19 : Set return address byte in CMOS
1A : Set temporary stack
* Protected made test and determined memory size - Runs in protected mode to address all storage, check (MSW) for protected mode. Base memory size saved.
Memory size determined with planer & i/o parity disabled. Soft reset check for parity error.
1B : Segment address 01-0000 (second 64K)
1C : Set or reset 512 to 640 installed f1
* Protected mode test and memory size
1E : Set exp. memory size determined in CMOS
1F : Test address line 19-23
20 : Cause a shutdown
21 : Return 1 from shutdown
* Initialize and start CRT Cont. (6845) Test video r/w reset video enable signal select alpha mode (40*24 b&w) w/r patterns, check addressability.
Error : 1 long, 2 short beeps (port 80 not used)
22 : Enable video signal and set mode, display horizontal bar on screen,CRT lines interface test, sence ON/OFF transition of video enable and horizontal sync lines
23 : check for advanced video card
24 : go to next test
* 8259 Interrupt controller test - r/w interrupt mask register with ls and 0s
Enable interrupt, check for hot interrupt (not expected) Test interrupt mask regiters
25 : Check for hot interrupts
26 : Display 101 error
27 : Check the converting logic 106 error
28 : check hot NMI interrupts (error 107)
29 : Test data bus to timer 2 (error 108)
* 8254 timer checkout - verify that system (0) count correctly
2A : Do test (error 102)
2B : Too fast
2C : Too slow (error 103)
2D : Check 8042 for last command ecepted (error 105)
2F : Go to next test if warm start
30 : Set shutdown return 2
31 : Enable protected mode
33 : Next block of 64K
34 : Restore checkpoint
35 : Keyboard test
36 : Check your «AA» scan code
38 : Error - check 8042 working
3A : Initialize 8042
3B : Check for ROM in 2K blocks
3C : Check for IPL diskette drive
3D : Initialize floppy for drive type
3E : Initialize hard file
3F : Initialize printer
40 : Enable H/W interrupt if 80287
41 : System code @ segment code E000.0
42 : Exit to system code
43 : Go to boot loader diskette attachment test
81 : Build descriptor table
82 : Switch to virtual mode
F0 : Set data segment
F1 : Interrupt test (programming interrupt 32)
F2 : Exceptional interrupt
F3 : Verify 286 LDT/SDT, LTR/STR
F4 : Verify 286 bound instruction
F5 : Verify push and pop all intruction
F6 : Verify access rights function
F7 : Verify ARPL functions
F8 : Verify LAR function
F9 : Verify LSL instruction
FA : Low meg chip select test

POST Codes - IBM PS/2 BIOS

00 : CPU self test
01 : 32 bit CPU register test, setup system timer
02 : System ROM checksum
03 : Test system enable/setup port
04 : Test system POS register
05 : Test Adapter setup port
06 : Test RTC/CMOS shutdown byte
07 : Test extended CMOS location
08 : Test DMA & page register 8 channels
09 : Initialize DMA command & mode registers
0A : Test refresh
0B : Test keyboard controller buffers
0C : Keyboard controller self test
0D : Keyboard controller test continuation
0E : Keyboard self test error
1F : Setup system memory configuration
10 : Test first 512K RAM in real mode
11 : Half system if memory test error
12 : Verify LGDT/SGDR LIDT/SIDT
13 : Initialize programmable interrupt controller #1
14 : Initialize programmable interrupt controller #2
15 : Initialize A20 interrup vectors
16 : Initialize 16 interrup vectors
17 : Check power RTC/CMOS power good signal
18 : Check RTC/CMOS checksum
19 : RTC/CMOS lost power
1A : Skip memory test in protected mode if warm reset
1B : Prepare for shutdown
1C : Setup stack pointer point to the end of first 64K
1D : Decide low memory size in protected mode
1E : Save memory size detected
1F : Setup system memory split address
20 : Check for extended memory beyond 64mb
21 : test memory address bus lines
22 : Clear parity error and channel check
23 : initialize interrupt 00
24 : Determine CMOS validity
25 : Write keyboard controller command byte
40 : Check valid CMOS and video
41 : Display error code 160
42 : Test PIC #1 & PIC #2 registers
43 : Test PIC #1 & PIC #2 registers with another pattern
44 : Check for interrupt with interrupt masked
45 : Test NMI
46 : NMI test error
47 : Test system timer 0
48 : Check stuck speaker clock
49 : Test timer 0 count
4A : Test timer 2 output
4B : Check if timer interrupt occurred

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ACCESS

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4C : test timer 0 for count too fast or slow
4D : Verify timer 0 interrupt
4E : Check 8042 ready for command
4F : Check for soft reset
50 : Prepare for shutdown
51 : Start protected mode test
52 : Test memory in 64K increments
53 : Check if memory test done
54 : Shutdown system and return to real mode
55 : Test for manufacture or regular test
56 : Disable keyboard
57 : Check for keyboard self test
58 : Keyboard test passed
59 : Test keyboard interface
5A : Configure mouse
5B : Disable mouse
5C : Initialize interrupt vectors
5D : Initialize interrupt vectors
5E : Initialize interrupt vectors
61 : Reset floppy drive
62 : Floppy drive test
63 : Turn floppy motor off
64 : Serial port setup
65 : Enable real time clock interrupt
66 : Configure floppy drives
67 : Configure hard drive
68 : Enable system CPU arbitration
69 : Scan for optional ROMs
6A : Verify serial & parallel ports
6B : Setup equipment byte
6C : Setup configuration error
6D : Set keyboard typematic rate
6E : Reset page register, boot up system

POST Codes - OLIVETTI PS/2 Compatible BIOS

01 : Processor test
02 : Shutdown
03 : Interrupt controller initialization
04 : Refresh test
05 : CMOS periodic interrupt test
06 : Timer ratio, CMOS vs. Refresh
07 : Test first 64K RAM
08 : Test the KBC 8742
09 : NMI test
0A : 8254 test
0B : Port 94h test
0C : Port 103h test
0D : Port 102h test
0E : Port 96h test
0F : Port 107h test
10 : Blank the screen
11 : KB/AUX device fuse check
12 : CMOS battery test
13 : CMOS RAM checksum test
14 : Extended CMOS checksum 0-8K
15 : System board and adapter initialization
16 : RAM test and initialization
17 : Protected mode register test
18 : CMOS RAM shutdown byte test
19 : 80286 protected mode test
1A : Video option ROM scan
1B : EPROM checksum test
1C : Interrupt contoller #1 test
1D : Interrupt contoller #2 test
1E : Interrupt vector initialization
1F : CMOS RAM test
20 : Extended CMOS r/w test
21 : CMOS clock test
22 : Clock calendar test
23 : Dummy checkpoint
24 : Watchdog timer test
25 : Test RAM from 64K to 640K
26 : Configure memory 640K

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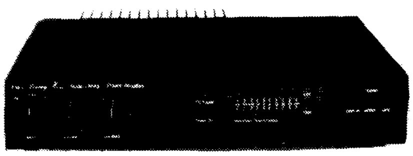

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1992/94 248 Pages. 247 x 190.

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1992 168 Pages. 217 x 138. 64 line drawings.

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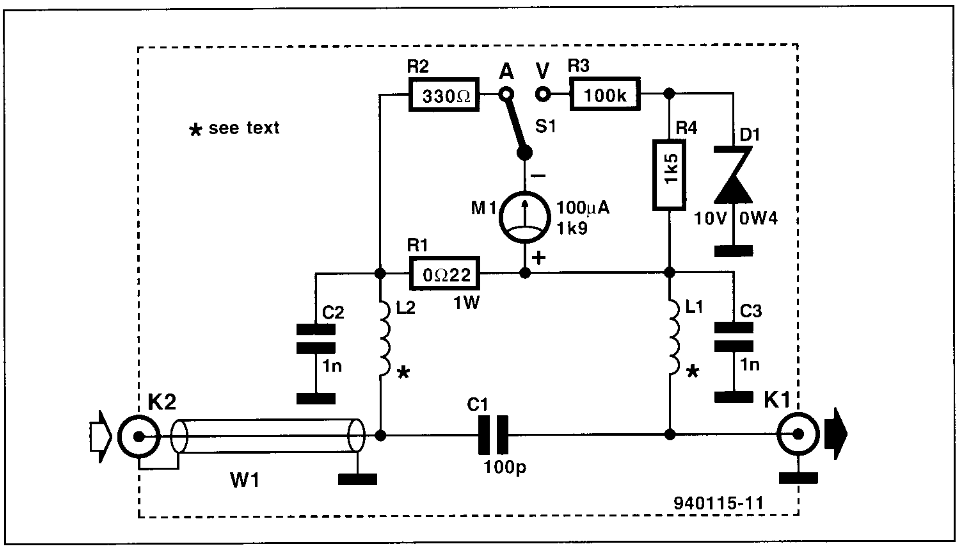


MOST low-noise converters (LNCs or LNBs) for satellite TV reception require either a fixed supply voltage of +15 V or one which is switched between +13 and +15 V. This voltage is supplied by the tuner, via the coax cable. The LNC current consumption is typically between 100 mA and 400 mA. The low-cost V/A tester described here allows you to detect short-circuits in the coax cable, and faults in the tuner. The little instrument has a current range of 0-1 A and a voltage range of 10-20 V.

The tester is inserted into the downlead coax cable between the LNC and the tuner with the aid of F-type sockets K_1 and K_2. K_1 is the LNC side, while the tuner is connected to K_2 via a short piece of coax cable. F-type plugs and sockets are generally available from satellite TV installers and retailers.

Capacitor C_1 provides d.c. insulation, but passes the RF signal on the downlead coax (950-2050 MHz). RF chokes L_1 and L_2 block the RF signal for the rest of the circuit, while C_2 and C_3 decouple the d.c. side for high-frequency signals. To prevent undue amounts of stray capacitance and inductance in the circuit (causing signal loss), capacitor C_1 and the two chokes must be connected with the shortest possible leads. For the very same reason, a piece of 75-Ω coax, W_1, is used to bridge the distance between K_1 and C_1. The d.c. path is terminated by shunt resistor R_1. The indicated 1-watt type is capable of handling a maximum continuous current of 2 A. Fortunately, most satellite TV tuners limit the LNC short-circuit current to a much lower value. In some low-cost tuners, the LNC supply fuse blows, and will need to be replaced (after remedying the cause of the fault).

With the switch, S_1, set to the 'A' (ampère) position, the moving coil meter, M_1, is connected in parallel to R_1. A series resistor, R_2, then limits the full-scale deflection of the meter to an effective current of 1 A.

For voltage measurements, the switch is set to the 'V' position. Since a range of only 10 V to 20 V is required, the voltage across the measurement network and its series resistor, R_3, is reduced by 10 V with the aid of zener diode D_1. The voltage across R_4 then equals the LNC supply voltage minus the 10-V zener voltage.

Construction hints

The LNC V/A tester should be housed in a small metal enclosure, preferably diecast, for which panel-mount F sockets are available. The RF chokes consist of about 7 turns of 0.5-mm dia. (24SWG) enamelled copper wire, close-wound, with an internal diameter of about 3 mm. No core or former is used. The construction allows large tolerances, since L_1 and L_2 serve as RF blocking devices only.

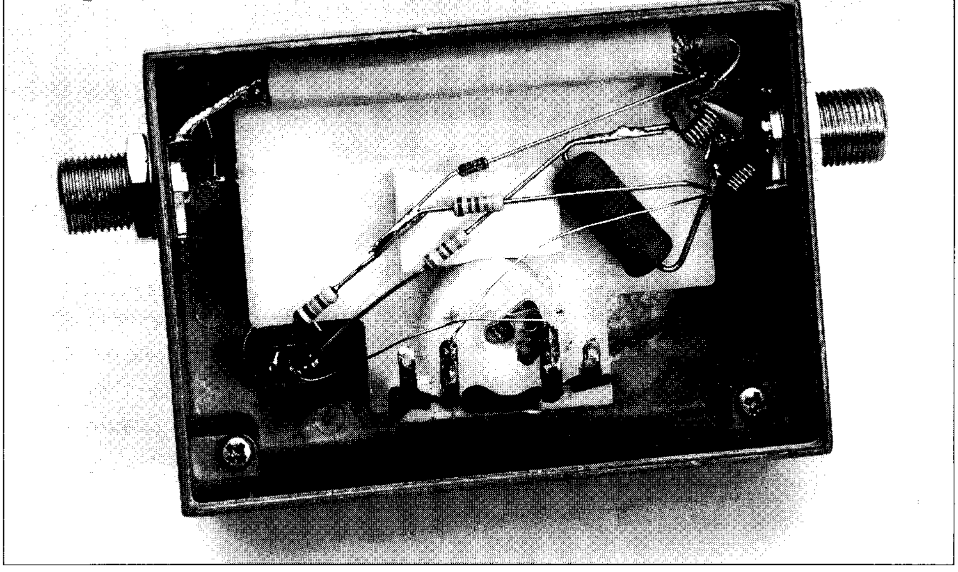
Components C_1, L_1 and L_2 should be fitted as close as possible to the centre pin of F socket K_2. The connection to the other F socket, K_1, is made via a short piece of 75-Ω coax cable. The screening at both ends of this short transmission line is connected to the ground contacts of the respective F socket. C_2 and C_3, too, must be connected with the shortest possible leads between the 'earthy' side of the chokes and ground.

For the rest of the circuit, 'flying wire' as well as 'stripboard' constructions may be used.

If you happen to have a moving coil meter with a different sensitivity than indicated in the circuit diagram, resistors R_2 and R_3 need to be altered to match the f.s.d. (full-scale deflection) current. In case of a short-circuit, resistor R_1 carries a current of 1 A, causing a voltage drop of 220 mV. This voltage should be made to correspond to the meter's f.s.d. current. That is achieved by the meter's coil resistance plus the value of R_2.

The value of R_4, finally, is computed from the maximum voltage which occurs across R_3 (10 V), and the f.s.d. current of the meter you wish to use. A possibly simpler way to arrive at the correct resistance values is to fit a preset and just measure out the required resistance. (940115)

Design by G. Kleine



1-TO-3-PHASE CONVERTER

Final part - Construction

Design by B. Yahya

Since the voltages existing in many parts of the converter may be lethal, great care must be taken in the construction of the converter. Not only should the usual safety guidelines be rigidly adhered to, but there should also be no use made of cheap, often untested, components. It is also strongly advised to use an isolating mains transformer during the construction and testing.

The printed-circuit board shown in **Fig. 5** is double-sided and through-plated and therefore not easily made without the proper tools and equipment.

Start by fitting all passive components, the transformers and the IC sockets on the board. Note that C_4 is fitted at the track side. Cover the tracks beneath C_{26} with insulating tape. Then fit regulators IC_{17} and IC_{18}. Connect the mains to the board and check that potentials of +12 V and +5 V exist at the outputs of IC_{17} and IC_{18} respectively. Next, verify that the +5 V line is available at all points indicated in **Fig. 3**. Do not insert the meter prod into the IC socket pins, since that damages the sockets beyond repair.

If all voltages are correct, switch off the mains and mount IC_1, IC_2, IC_3, IC_4 and IC_5. Switch on the mains again and check that there is a signal of 1 MHz at pin 1, and PWM signals at pins 2, 3 and 4, of IC_5. If these signals are absent, the processor is not working properly. In that case, check all previous work thoroughly.

Interconnect K_2 and K_4, and verify that the PWM signals on pins 2, 3, and 4 of IC_5 vary when P_5 is turned. These signals should also be present at the six outputs of IC_5,

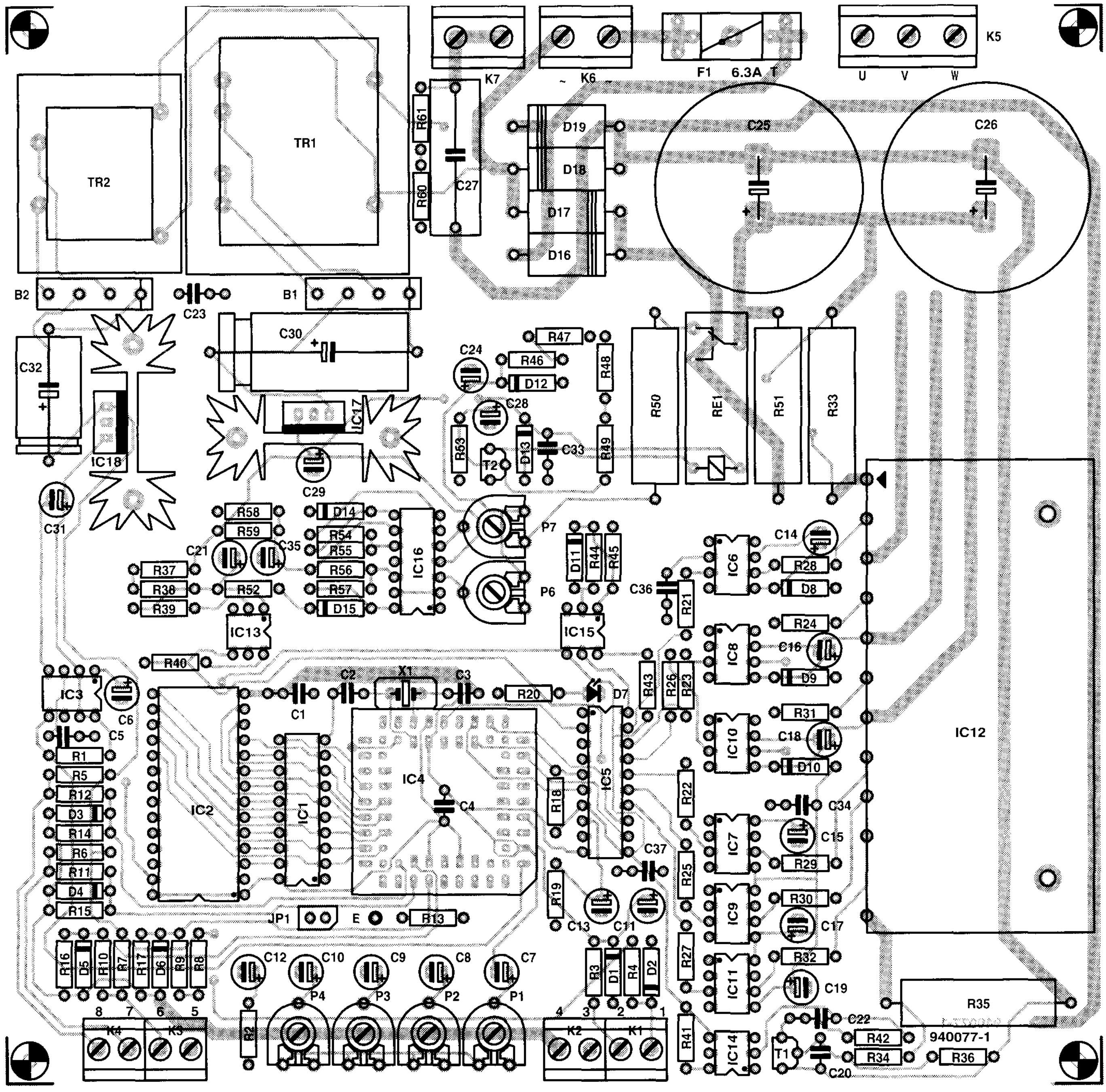


Fig. 5. Printed-circuit board for the 1-to-3-phase converter – see also pages 75 and 76.

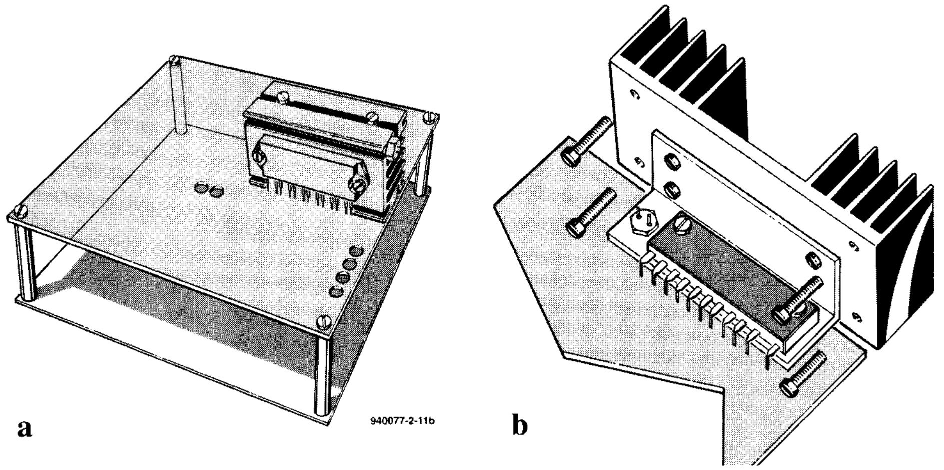


Fig. 6. There are two ways of fitting the main heat sink.

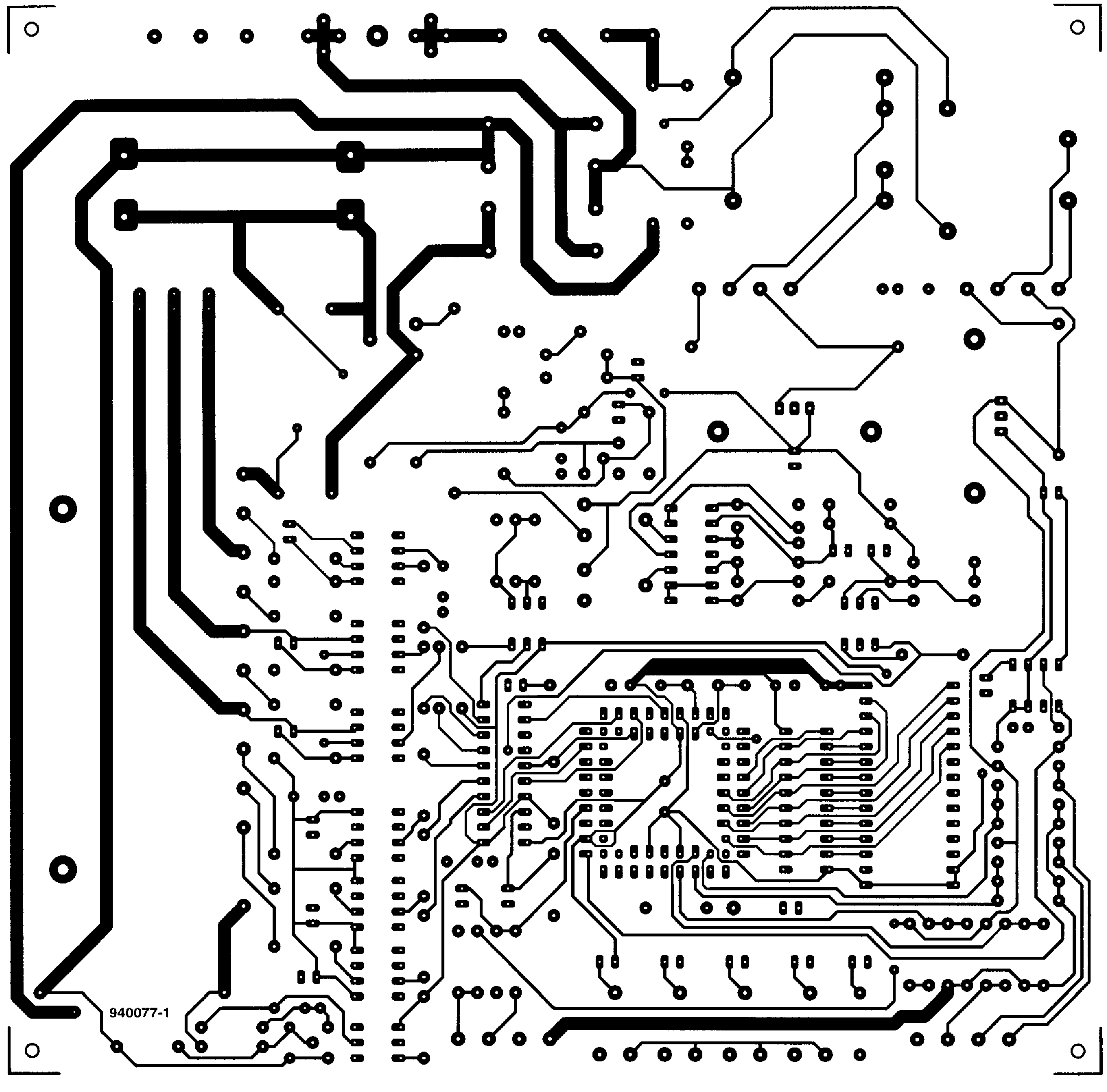
provided D_7 does not light. This LED may be made to light by interconnec-ting pins 4 and 5 of IC_{13}, IC_{14} or IC_{15}. It will extinguish (after about 4 seconds) when the links between K_2 and K_4 and pins 4 and 5 of the relevant optoisolator have been removed. Switch off the mains.

Mount the remaining semiconductors and integrated circuits. Note that like normal MOSFETs the IGBT module is vulnerable to static electricity.

If motors ≤100 W are to be used, there is no need for a heat sink for IC_{12}; at higher powers, this is a must. There are two ways of cooling, which are illustrated in **Fig. 6**; which of these is chosen depends on the application of the converter.

In **Fig. 6a**, the IGBT, mounted on a heat sink which also houses the NTC, is at right angles to the board. If the motor (or other load) is rated at ≥300 W, a 3 mm thick aluminium sheet of the same size as the board is fixed above the board: at one side directly to the heat sink and at the other side via two spacers. Drill suitable holes in this sheet to retain access to the presets.

In **Fig. 6b**, the IGBT is bent slightly and mounted on the board with a (300 mm)



wide piece of aluminium, bent at right angles, sandwiched between them. Make sure that none of the tracks is touched. Moreover, the aluminium angled sheet should be at a distance of ≥3 mm from R_{35} and the tracks to K_5. Use heat conducting paste liberally. Next, screw a heat sink of ≤2 K W^{-1} (SK04) to the aluminium. Finally, mount the NTC on the heat sink as close as possible to the IGBT.

The finished board must be fitted in a metal enclosure, which allows at least 3 mm space between it and the board. The enclosure must, of course, be earthed in accordance with safety regulations (in the UK, this should be the mains earth) see **Fig. 7**.

Connect the open-circuit converter to the mains and switch this on, whereupon the relay should be actuated. Check that there is a voltage of about 340 V on C_{25}. When the mains is switched off, this po-

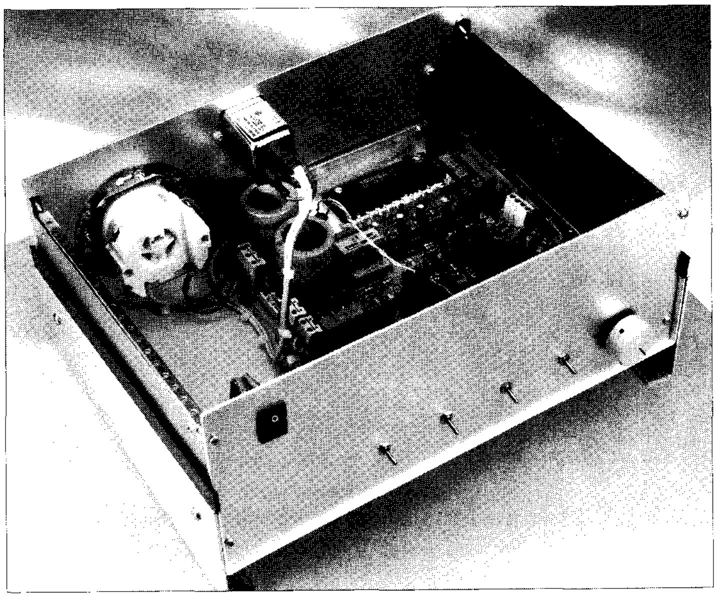
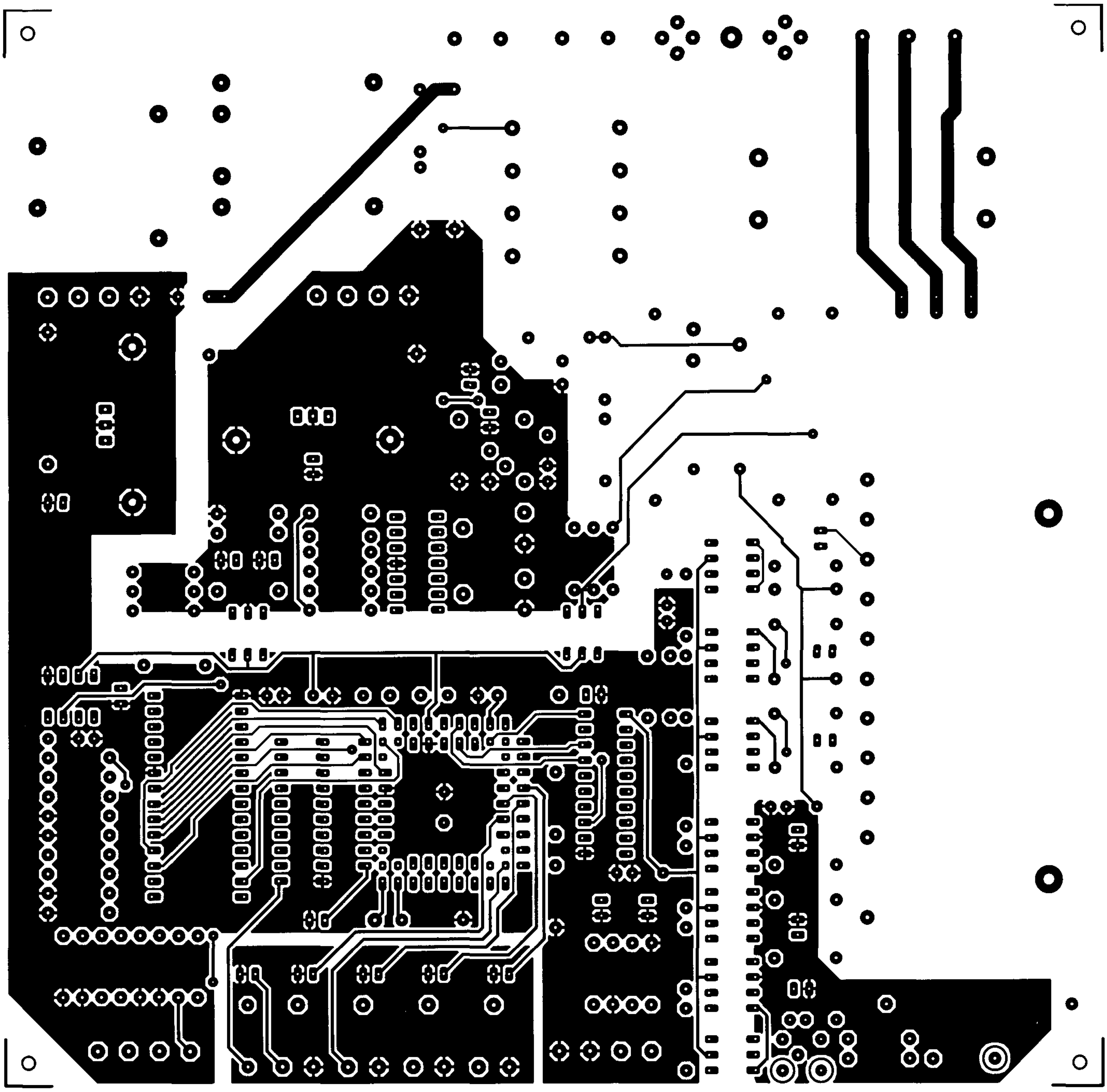


Fig. 7. The converter in its (earthed!) metal enclosure.



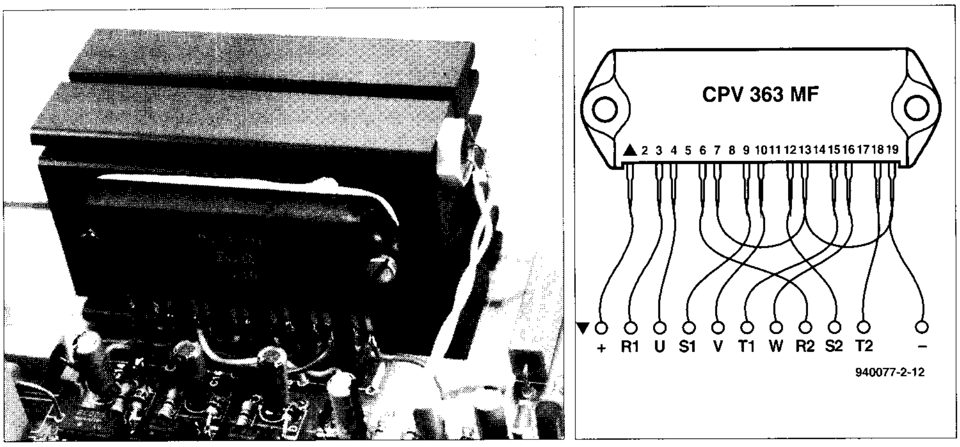


Fig. 8. How to fit the IGBT from International Rectifiers.

tential should disappear within 5–6 s.

The board is designed for an IGBT Type MP6750 from Toshiba. If this is difficult to obtain, International Rectifiers' Type CPV363MF may be used. Since this is not pin compatible with the Toshiba module, some pins have to be linked to the board with short lengths of wire as shown in **Fig. 8**.

If a Variac™ (variable transformer) is available, supply the mains via this and adjust it to give a potential of 270 V across C_{26}. Adjust P_7 to cause the level at pin 4 of IC_{16d} changes from high to low. Then, adjust the Variac to give a potential of 360 V across C_{26} and adjust P_6 to cause the level at pin 8 of IC_{16c} to change from low to high.

If a Variac is not available, measure the potential across C_{26} and C_{35}. Turn P_6 until the voltage at its wiper is $(U_{C26}/360)\ U_{C35}$ volts. Adjust P_7 until the voltage at its wiper is $(U_{C26}/270)\ U_{C35}$ V. Remobve the Variac and connect the mains directly to the converter.

If a temperature gauge is available, check that the thermal protection is actuated when the temperature reaches 80–85 °C.

Connect a three-phase motor to the converter and switch on the mains. The motor earth should be connected to the mains earth (standard in UK). Set all potentiometers, other than P_6 and P_7, to the centre of their travel and link K_2 to K_4. The motor should then gradually begin to run. Set the rotational speed with P_5. If the motor switches off or on too quickly, this may be remedied by varying P_4 and P_3 respectively. Finally, set P_1 (motor runs clockwise) and P_2 (motor runs anticlockwise) as desired.

When the converter is used close to vibrating parts (such as the motor itself), it is advisable to fix any parts that may be set into vibration (crystals, capacitors) in place with heat-resistant glue.

When one of inputs 1–4 (pins 5–8 of K_3 and K_4) is enabled and the mains is switched on, the converter goes into an error state, indsicated by the lighting of D_7 (when the output can not be made active). This state is removed by earthing the relevant input, whereupon D_7 extignuishes and the output may be actuated again.

A final note: since PWM signals are used, it is not possible to measure the output voltage with a multimeter. A true-r.m.s. meter or oscilloscope must be used instead. The voltage between two phases may be 220 V.

Parts list

Resistors:
R_1, R_{34}, R_{37} = 560 Ω
R_2 = 82 Ω
R_3, R_4 = 2.2 kΩ
R_5–R_{12}, R_{59} = 5.6 kΩ
R_{13}–R_{17} = 3.3 kΩ
R_{18} = 470 Ω
R_{19} = 330 Ω
R_{20} = 680 Ω
R_{21}–R_{23}, R_{25}–R_{27}, R_{53}, R_{54}, R_{56} = 1.2 kΩ
R_{24}, R_{28}–R_{32} = 33 Ω
R_{33}, R_{35} = 0.18 Ω, 5 W
R_{36} = 120 Ω
R_{38} = 120 Ω
R_{38} = NTC, 4.7 kΩ
R_{39} = 270 Ω
R_{40} = 120 kΩ
R_{41} = 10 kΩ
R_{42} = 470 Ω
R_{43} = 10 kΩ
R_{44} = 180 Ω
R_{45} = 100 Ω
R_{46}, R_{48}, R_{49}, R_{55}, R_{57} = 220 kΩ
R_{47} = 180 kΩ
R_{50} = 10 kΩ, 5 W
R_{51} = 47 Ω, 5 W
R_{52} = 1 kΩ
R_{60}, R_{61} = 470 kΩ
P_1–P_4, P_6, P_7 = 25 kΩ preset
P_5 = 10 kΩ linear potentiometer

Capacitors:
C_1, C_5, C_{23}, C_{33}, C_{34}, C_{36}, C_{37} = 100 nF
C_2, C_3 = 27 pF
C_4 = 100 nF
C_6, C_{13} = 1 μF, 16 V, radial
C_7–C_{11}, C_{21} = 4.7 μF, 16 V, radial
C_{12}, C_{14}–C_{19}, C_{24}, C_{28}, C_{35} = 10 μF, 16 V, radial
C_{20} = 470 pF
C_{22} = 4.7 nF
C_{25}, C_{26} = 220 μF, 400 V, radial
C_{27} = 15 nF, 1500 V
C_{29}, C_{31} = 22 μF, 16 V, radial
C_{30} = 1000 μF, 25 V
C_{32} = 470 μF, 25 V

Semiconductors:
D_1 = zener, 5.1 V, 400 mW
D_2 = zener, 6.2 V, 400 mW
D_3–D_6 = zener, 4.7 V, 400 mW
D_7 = LED
D_8–D_{10} = BYT11 or BYV36E (1000 V, 150 ns)
D_{11}, D_{13}–D_{15} = 1N41448
D_{12} = zener, 12 V, 400 mW
D_{16}–D_{19} = FR606 (500 V, 5 A)
B_1 = rectifier bridge B250C1500
B_2 = rectifier bridge B40C1500
T_1 = BC547B
T_2 = BC337

Integrated circuits:
IC_1 = 74HCT573
IC_2 = EPROM Order No. 946640-2*
IC_3 = TL7705A CP (Texas Instruments)
IC_4 = 80C535 (Siemens)
IC_5 = GAL Order No. 946640-1*
IC_6–IC_{11} = PC923 (Sharp)
IC_{12} = MP6750 (Toshiba) orCPV363 MF (International Rectifier) see text
IC_{13}–IC_{15} = CNY17-4 (Siemens)
IC_{16} = LM324
IC_{17} = 7812
IC_{18} = 7805

Miscellaneous:
JP_1 = 2-way jumper
K_1–K_4 = 2-way terminal block, pitch 5 mm
K_5 = 3-way terminal block, pitch 7.5 mm
K_6, K_7 = 2-way terminal block, pitch 7.5 mm
X_1 = crystal, 12 MHz
F_1 = fuseholder and 6.3 A slow fuse
Re_1 = relay, one change-over contact, coil 12 V
Tr_1 = mains transformer, 12 V, 3 A, e.g. Velleman 1120038M (Maplin)
Tr_2 = mains transformers, 12 V, 1.5 A, e.g. Velleman 1120018M (Maplin)
1 off mains switch, 3 A, with indicator
2 off heat sink, SK104 (37.5 mm high)†
1 off heat sink SK68 (75 mm high) or SW40/30 (100 mm high) with SK04† (see text)
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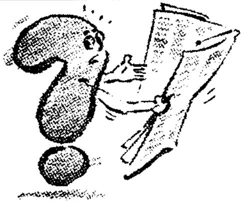

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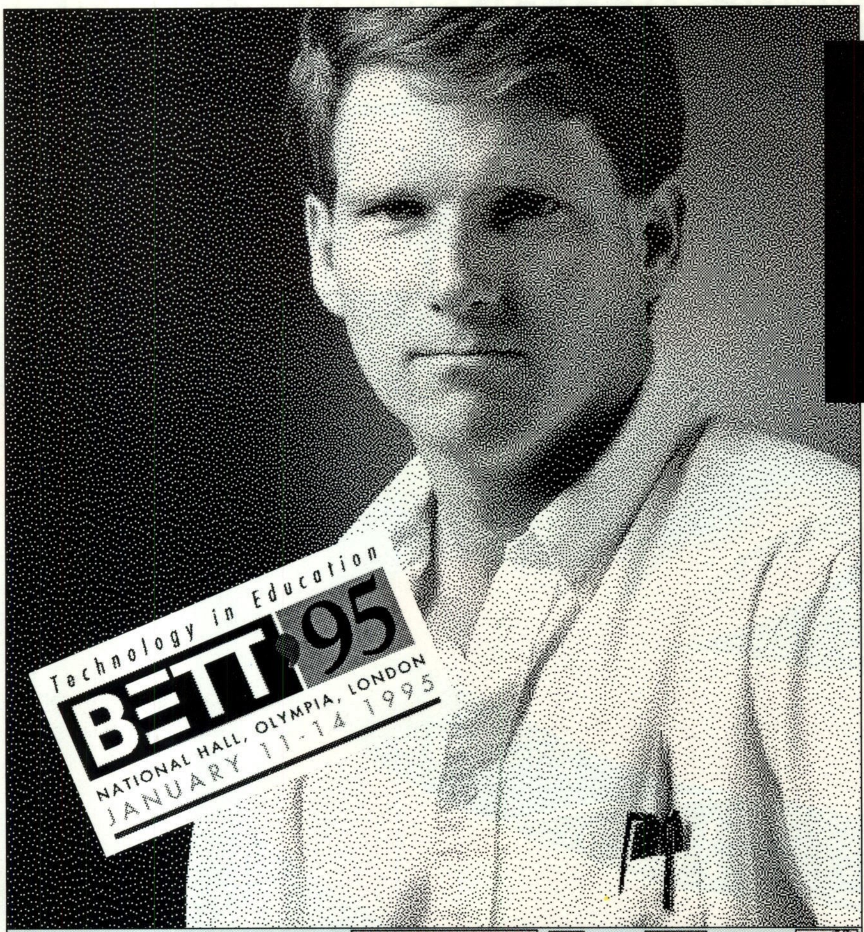

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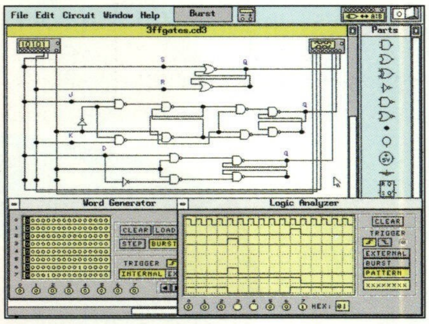

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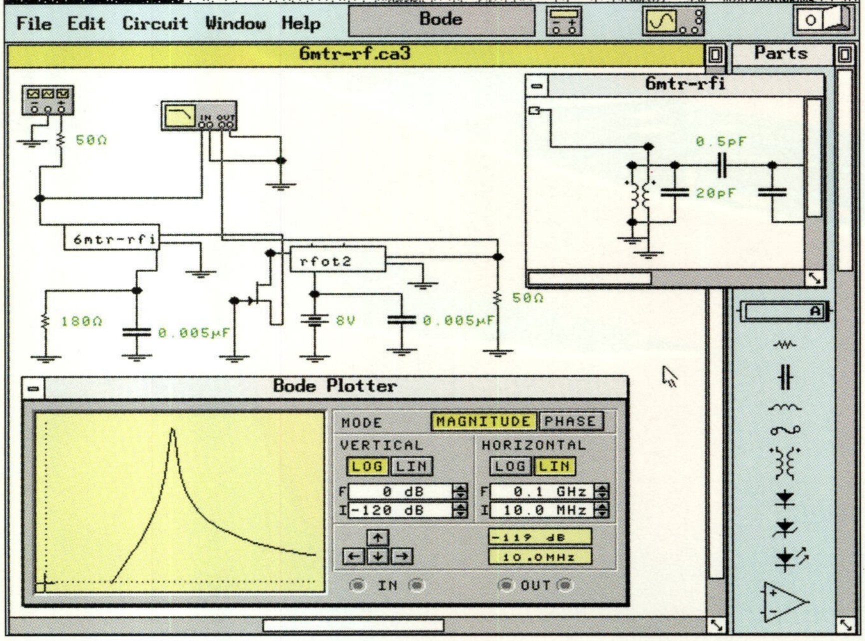

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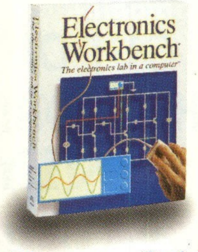

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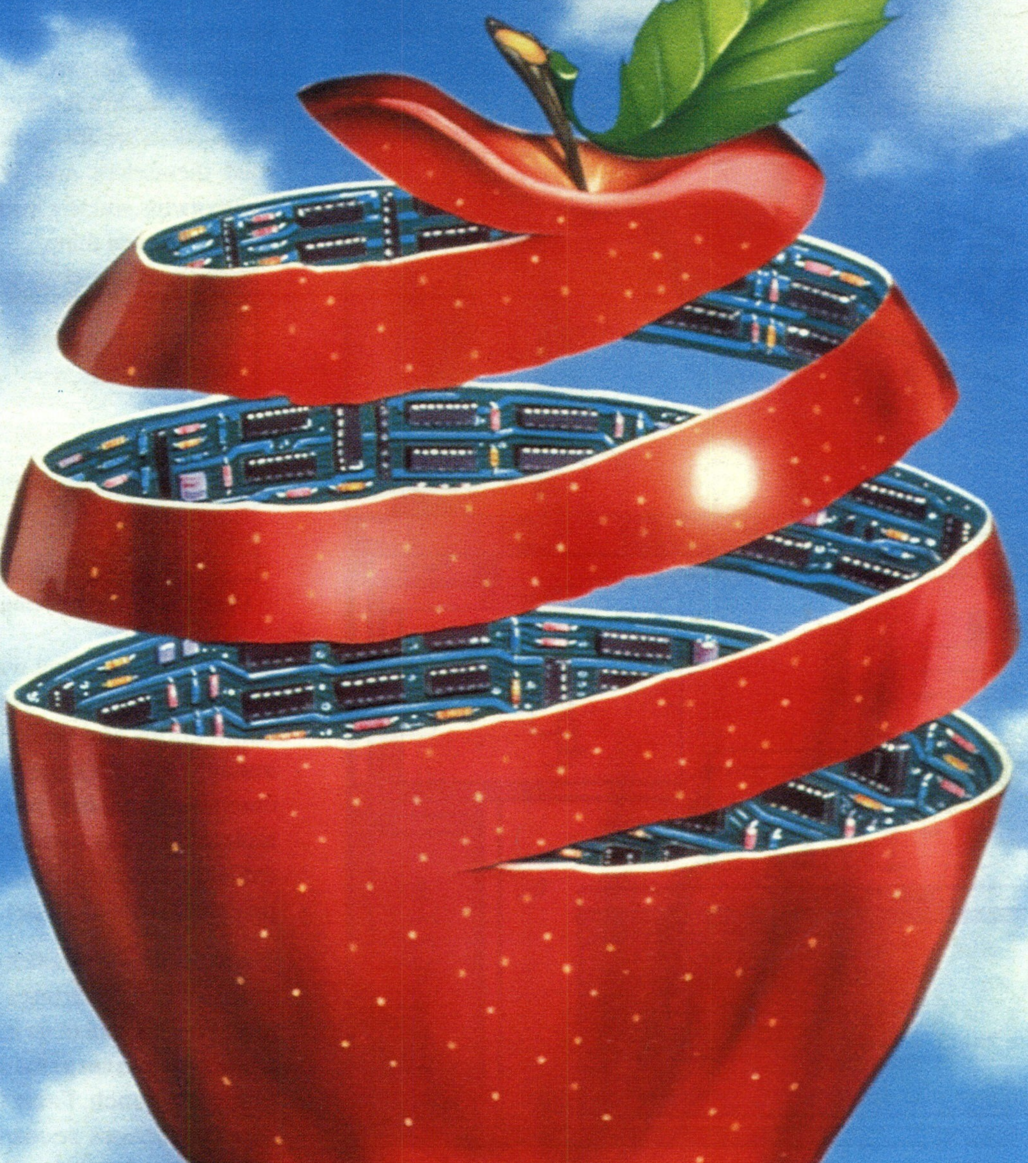

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